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A Review of 1-Bit Full Adder Design Using Different Dynamic CMOS Techniques

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***Abstract*-- The Domino CMOS Logic Circuits are famously utilized in Very Large Scale Integrated (VLSI) structure. To design a VLSI circuit having low power and fast execution or high speed is the most testing task. By and by, one of the main goals is low power VLSI circuits with high speed. Full Adders are mainly used in various circuits which can perform various errands like development, duplication, division etc. In this manner it will diminish the force usage in full adders expects an enormous part of VLSI circuits having low power. In this paper, domino logic is used to manage a stable, particularly improved response for two constraints in full adder circuits i.e. power and delay. We review the Power, Delay and Power Delay Product (PDP) of 22T Domino Full Adder, 27T Domino Full Adder and 28T Static Full Adder. In this we also review these 3 circuit on the basis of different technology nodes or the feature length i.e. 45nm, 90nm and 180nm.**

***Keywords*: Domino, CMOS, Adder**

I. INTRODUCTION

The current power consumption of the circuit is increasingly increasing due to the continuous rise in chip complexity and the number of semiconductor transistors. Moreover with the development in no. of advantageous devices, just like PCs and phone's low power and quick circuits or high speed become critical. The full adder is a fundamental component of many circuits that perform operations such as comparator, parity checker, and compressor etc. With the need of low power and high speed processors and the usage of reduced devices have achieved astoundingly brisk advancement in VLSI circuit designs. Full adder circuit is fundamental to most developed circuits that perform extension or allowance [1,3]. It is assumed that it incorporates two parallel digits, notwithstanding a pass on in digit to make an entirely and do digit. It go probably as a basic segment of various circuits especially used for performing calculation errands, for instance, comparator, equality checker and so on. For arranging a complete adder, there are two main logic approaches i.e. static and dynamic [1].

A. Static/ Steady-State Logic:

Static logic circuits are used to implement static logic circuits in a versatile manner. Static, or steady-state based logic functions, simple CMOS structure action, or, in other words,[4] combinational circuits are widely used. As long as the power supply is supplied,

II. LOW POWER FULL ADDER DESIGN

In any CMOS circuit there are many sources of consuming power.[1]

1) During output transitions there is output switching which leads to switching power consumption.
2) Static power consumption due to static current & leakage.
3) Transistor switching due to current flow from VDD to GND leads to Short circuit power consumption.

In full adder CMOS circuits, to reduce power consumption.

1) To reduce dynamic power, minimize the input and output capacitances.
2) To reduce static and short circuit power, avoid using VDD and GND both simultaneously.
3) To reduce power consumption in circuits, use pass transistors in circuit to reduce the no. of transistor count and hence power.
4) To minimize the conduction of transistors, use variable W/L ratio

a typical static logic gate can generate its output levels. It consists of a PULL UP, which is a network of P transistors, and a PULL DOWN, which is a network of N transistors. When the P network is turned on, output rises to Vdd supply voltage, and when the N network is turned on, output falls to Gnd.

The basic characteristics of the Static CMOS logic are:-

- Very low dissipation of static power.
- High margins for noise (full rail to rail swing).
- Low output impedance, high impedance of input.
- No steady state route between GND &VDD.
- The load capacitance and transistor resistance determine the delay.
- Equivalent times of increase and fall.

The speed of the static CMOS circuit is dependent on the size of transistors and the numerous parasites that are implicated by it. The issue with this form of the implementation is that for N fan-in-gate 2N no. of transistors are needed i.e. more area is needed for logic implementation. This affects the speed and capacitance of the gate.

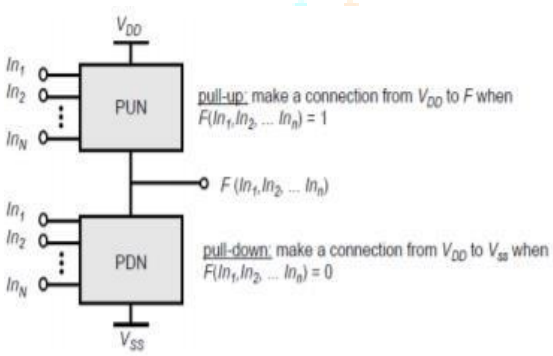

Fig 1 Generalized static CMOS Logic

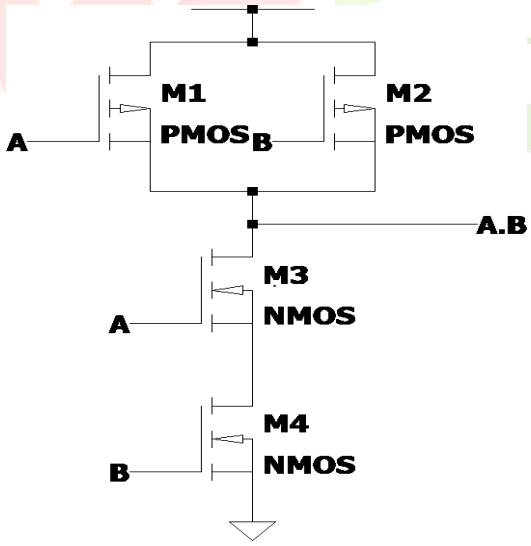

Fig2NAND logic using static CMOS

B. Dynamic Logic:

In high-density, high-performance digital applications where reducing circuit delay and silicon area is a major goal, dynamic logic circuits offer a number of significant advantages over static logic circuits. A clocked pull-up transistor is used by the dynamic circuit rather than a PMOS that is always ON.[4] The operation of all dynamic logic gates depends on temporary charge storage in parasitic capacitance. This operational property involves periodic updating of internal node voltage levels, as the stored charge can't be held indefinitely in the condenser.

Pre-charge

At CLK=0, the output node Out is preloaded to VDD by transistor PMOS. During this period of time, the evaluation and NMOS transistor is OFF, such that the pull-down route is disabled. The FET at evaluation time removes any static power that would be consumed during the pre-charge time (i.e., if both the pull-down and the pre-charge system were switched on simultaneously static current would flow between the supplies).

Evaluation

At CLK=1, the pre-charge transistor is off and evaluation transistor is ON. The result is conditionally discharged depending on the values of the input and topology for the pull-down. When the inputs are such that the inputs are PDN conducts, so there is a low resistance route between OUT and GND and output is discharge to the GND.

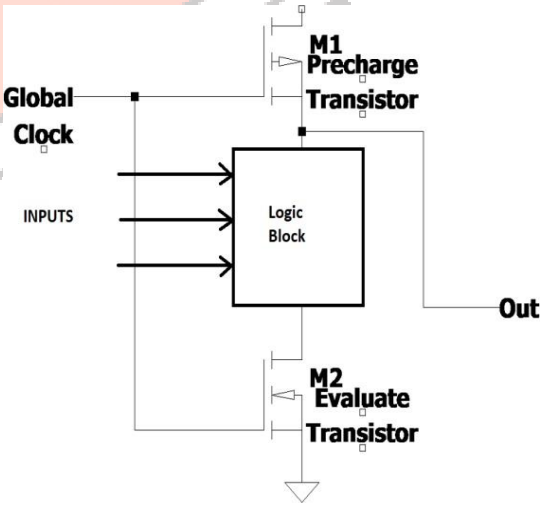

Fig3 Generalized Dynamic Logic Circuit

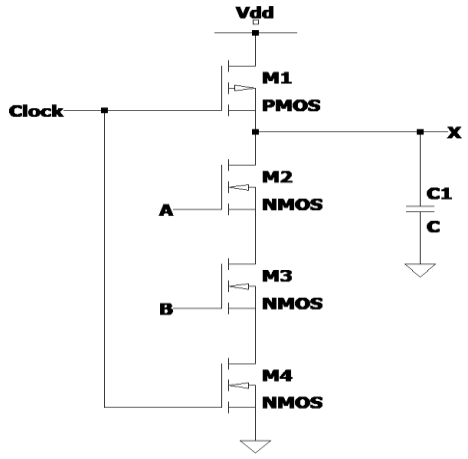

Fig4 2 input NAND using Dynamic Logic

III. 1-BIT FULL ADDER

Full adder structures are used as a major and essential squares to gather any VLSI and embedded applications. So it demands the authorities to setup low power and low speed full adder circuits to improve adequacy of the arrangement. This task manages a plan of 1-bit crossover adder circuit by joining CMOS and transmission gate logic. [1]

Limits of plans like deferral and power are assessed and power delay thing are arranged and are differentiated and the prior works that joins CMOS logic, CPL, TGA and TFA. Power use is found to be diminished and delay also diminished phenomenally. Moreover all the adders which are arranged from past composed works and proposed full adder circuits are placed in a 2-digit comparator autonomously and execution of 2-cycle comparator will be inspected.[17] The comparator arranged with proposed full adder circuit shows less power and diminished delay, from now on better power concede thing appeared differently in relation to others.

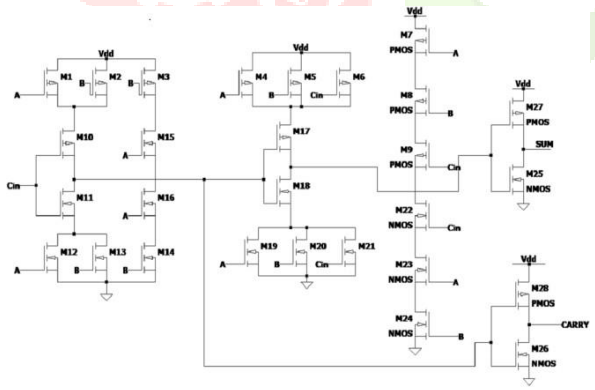

Fig51-bit Full Adder Cell

IV. CONCEPT OF DOMINO LOGIC

Domino logic is a CMOS-based advancement of the dynamic logic methods subject to either PMOS or NMOS semiconductors. It allows a rail-to-rail output swing. The Dynamic Domino, circuits work using a gathering of pre-charge and evaluation stages facilitated by the system check signal as in Fig. The domino logic incorporates the utilization of simply the NMOS logic when appeared differently in relation to the static CMOS circuits in PDN in view of which there is epic proportion of decrease in the amount of semiconductors in domino logic subsequently reducing the zone of the circuit.[6]

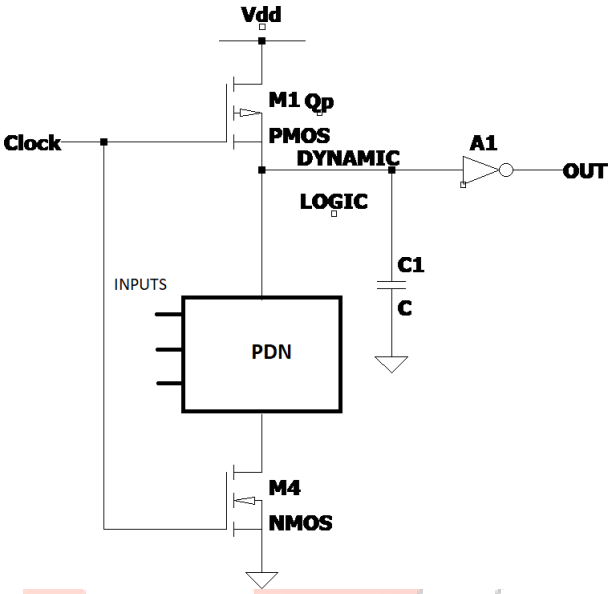

Fig6 Basic domino circuit

In the above figure CL addresses the parasitic capacitance and PDN addresses the draw down association which comprehends the logic ability to be completed. Exactly when the clock is low the circuit is in pre-charge stage and Q_p is on and Q_e is off. The dynamic network pre-charge to V_{dd} and the output of the CMOS buffer is low. At the point when CLK =1 the circuit is in evaluation stage, QE is on and QP is off. Right when the information mix achieve objective "0" at that point the dynamic network stays charged and output is low. Right when the information blend achieves reasoning "1" at that point the dynamic network are released to ground and the output of the CMOS inverter is high. At any rate these domino logic gates experience the ill impacts of lesser resistance and higher power dispersal. As the development scales back the spillage current increment and expects an essential capacity in the hard and fast power dispersing. [7]

A. STANDARD FOOTLESS DOMINO LOGIC FULL ADDER

The footless arrangement is depicted by the way that arrival of dynamic network is speedier. This property is misused by the world class circuits. The circuit of the SFLD logic is showed up in Fig. Movement of Footless-Domino is according to the accompanying: During the pre-charge stage, for instance exactly when the clock(CLK) is LOW, the dynamic network is charged to VDD and the guardian semiconductor goes ON to keep up the voltage of the dynamic network. [6]

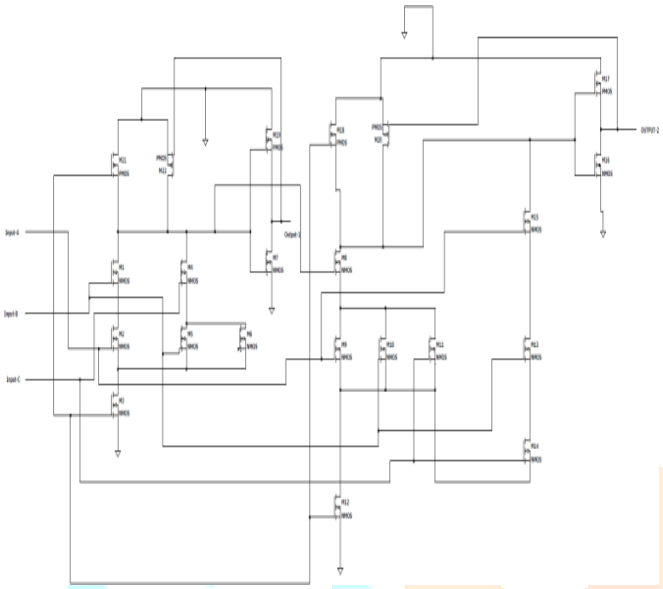

Fig7 Standard footless domino logic full adder

During the evaluation mode, for instance right when the CLK goes HIGH, the dynamic network is either released to ground or remains HIGH depending upon the data sources. However, the circuit suffers with colossal proportion of power dispersal.

B. STANDARD FOOTED DOMINO LOGIC FULL ADDER

The footer NMOS semiconductor is related with the beginning of evaluation NMOS semiconductor to get the FDL plan which basically diminishes the leakage current. Fig shows the most standard footed domino logic circuit. Right when CLK is LOW, the dynamic network is pre-charged to VDD. [10] In this stage the footed semiconductor is slaughtered, which diminishes the leakage current. Exactly when CLK goes HIGH, footer semiconductor is turned on. Thusly, dependent upon moving toward data to pull-down network, the state of output network is gained.

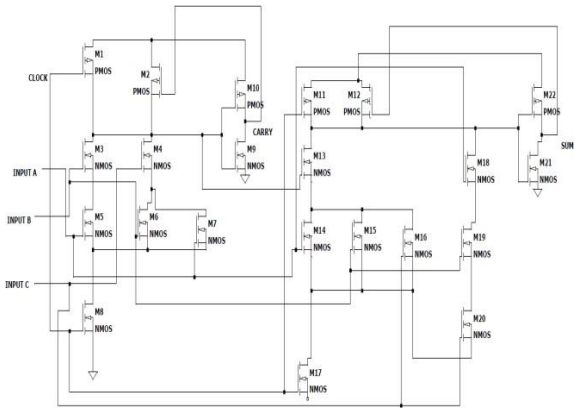

Fig8 Standard footed domino logic full adder

This footed circuit offers better power utilization with more slow speed and the no. of semiconductors is likewise increments than the past circuit.[10]

C. DUAL RAIL DOMINO LOGIC FULL ADDER

Dynamic domino gate have the extraordinary limitation of not having the choice to finish changing logic capacities (with reference to model, NOR, NAND, XOR) and high power use because of the clock. [6]To boost the speed of CMOS circuits, Dual Rail Domino Logic is used which is a type of pre-charged circuit.[10] A Dual Rail Domino full adder cell is shown in Fig. A domino gate has a CMOS circuit that is totally new, followed by a static CMOS circuit.

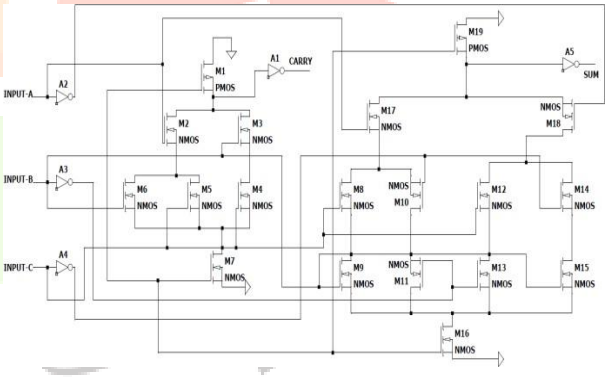

Fig 9 Dual rail domino full adder

One significant bit of the dynamic logic, pre-charged arrangement styles over the static styles is that they remove the false advances and therefore the relating power dispersal. Regardless, in exceptional circuits, the dispersal network and thus the clock signal drivers disperse additional power. This circuit uses less power and takes up less space than previous circuits, but it has the downside of requiring far more semiconductors.

D. HIGH SPEED DOMINO LOGIC FULL ADDER (Hs)

The circuit of the HS Domino logic full adder is showed up in Fig. In HS domino the guardian semiconductor is driven by a mix of the output network and a given clock. The circuit fills in as follows: Toward the start of the evaluation stage, when clock is high, MP3 and MP6 turns on and thereafter the gate semiconductors MP2 and MP5 slaughters. [10] Thusly, the conflict between evaluation network and operator semiconductor is diminished by turning off the guardian semiconductors close to the beginning of evaluation mode.[9]

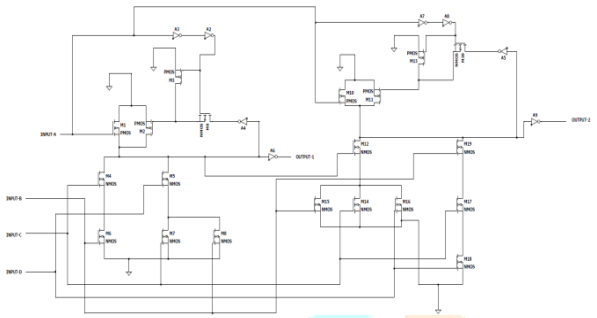

Fig 10 High speed domino full adder

As of now, if the dynamic node has been released to ground, for instance in the event that any data goes high, the NMOS semiconductors MN1 and MN2 stays OFF. Then again, if the dynamic node stays high during the evaluation stage, MN1 and MN2 turns on and pulls the gates of the guardian semiconductors. In this manner guardian semiconductors will go on to keep the dynamic node high, battling the impacts of leakage. It requires all the more no. of semiconductors than past domino adders, however gives less power utilization and better zone.

V. LOGIC APPROACHES OF DIFFERENT FULL ADDERS

A. 27T Domino Full Adder

In the segment, we consider a 27 semiconductors 1 cycle full adder circuit utilizing domino logic as appeared in fig. the result of full adder cell and C_{out} can be carried out utilizing transitional sign.[1]

$$\square = \overline{\square\square} \quad (1)$$

OR

$$\overline{\square} = \square \oplus \quad (2)$$

Thus, in this circuit we used a five semiconductors hooked in to XNOR entryway for arranging a full adder as showed up in figure, in this circuit there is no quick path among V_{dd} and Ground& arrival of semiconductor depends upon the clock signal.

In this circuit, when the clock is 0 it is a pre-charging stage now one among a sort hub is invigorate to V_{dd}, and when the clock is 1 referred to as evaluation stage. In this circuit, arranging XNOR entryway used Static reasoning yet while arranging the complete adder used a mixed style approach static similarly as domino reasoning style, the output of full adder depends upon the clock A,B,C inputs.

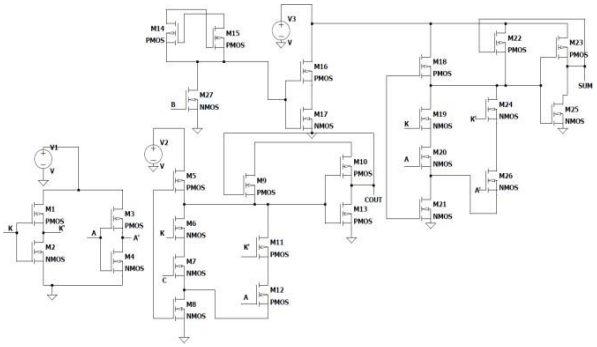

Fig 11 27 transistor 1-bit full adder (27T)

Power Delay Product has been determined from the equation below:-

*PDP = Power Average * Delay*(3)

B. 22T Domino Full Adder

In this segment we proposed a 1-cycle full adder circuit utilizing domino thinking technique as appeared in figure. Utilizing 22 semiconductors. In this circuit there is no speedy course among Vdd and GND and appearance of semiconductor rely on the clock signal. In the proposed plan, during pre-charging stage clock is center point and dynamic center is charged. During assessment stage check winds up being high .[1] In this game plan variable cutoff voltage procedure and different edge strategies are utilized, so the yield of the full adder won't swing out and it reduces the spillage current that thusly limit the force dispersal of the circuit.

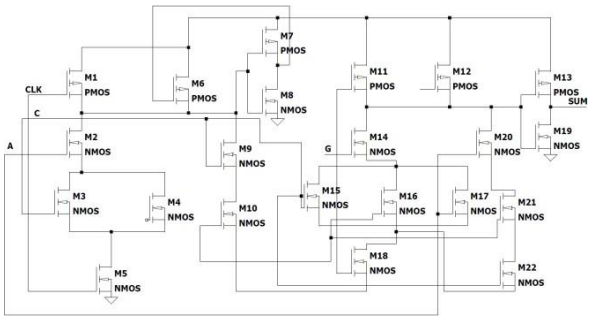

Fig 1222 transistors 1-bit full adder (22T)

Power Delay Product has been determined from the below equation:-

$$PDP = Power_{average} \times Delay \quad (4)$$

C. 28T Static Full Adder

The basic structure for 28T static 1-bit full adder, for any arithmetic circuit as shown below in the figure where A, B, C are inputs and Sum & Cout are outputs of this full adder. [1, 2], [8]

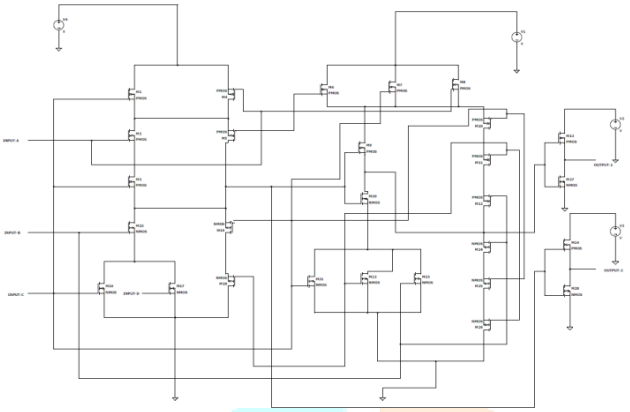

Fig1328 transistor 1-bit full adder (28T)

VI. CONCLUSION

From the study, it has been observed that the choice of Static Logic and Dynamic CMOS Logic depends upon the applications in which these circuits are required. For simplified implementation of logic, e.g. we can use static logic in NAND, NOR gates etc. Since they provide comparable performance at low cost and less complexity with respect to dynamic logic, though dynamic logic is preferable to complex logic circuit designs such as microcontroller. For comparative study of the analysis of static and dynamic CMOS circuits, a right and suitable choice of logic along with voltage variation can results to the design of low power and high performance VLSI chips.

In this current work, we are reviewing 22T, 27T and 28T Domino and Static full adders on the basis of Power, Delay and Power Delay Product (PDP). In general, the two variables that can't be reduced at the same time are power and delay, but these parameters can be optimized, so in the current work a suggested full adder based on domino logic approach 22T, the optimization of these two constraints are possible and the proposed design gives the best result in power dissipation and delay, [2] power delay product as compared to 28T, 27T full adder based on Static and Domino Logic approach.

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