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Design And Implementation Of Single-Ended 11t Sram Cell Using Finfet Technology

[1]D. Bhavana, [2]M. Saithi Sowmya, [3]K. Harika, [4]B. Yuva Chandana, [5]B. Lakshmi

[1]Under Graduate Student, [2]Under Graduate Student, [3]Under Graduate Student, [4]Under Graduate Student,
[5]Associate Professor,
[1]Electronics and Communication Engineering,
[1]Gayatri Vidya Parishad College of Engineering for Women, Visakhapatnam, India.

Abstract: In modern computing systems, Static Random-Access Memory (SRAM) is a crucial component used in cache memory and embedded applications. However, traditional 6T SRAM cells face challenges including increased power consumption, reduced stability, and susceptibility to noise—especially at lower supply voltages. To address these limitations, this project proposes the design and implementation of a Single-Ended 11-Transistor (11T) SRAM cell using 18nm FinFET technology. The cell introduces an additional NMOS transistor to improve read and write operations, while minimizing half-select disturbance and enhancing Static Noise Margins (SNM). The FinFET-based design enables better leakage control and reduced short-channel effects, making the SRAM cell highly suitable for low-power applications. A comprehensive simulation is carried out in Cadence Spectre, and performance is evaluated across key metrics such as Read/Write Delay, SNM, and power consumption. Comparative analysis with conventional 6T, 10T, SE10T, and ST10T SRAM cells reveals that the proposed 11T design offers superior performance in terms of energy efficiency, stability, and delay. The results confirm that the cell is robust for near-threshold voltage applications and scalable for future low-power VLSI designs.

Index Terms – SRAM, FinFET, Static Noise Margin, Low-Power Design, 11T SRAM Cell, Read/Write Delay, Memory Stability.

1. INTRODUCTION

Static Random-Access Memory (SRAM) plays a pivotal role in modern computing systems, especially in high-speed cache and portable embedded devices where power efficiency and reliability are critical. As technology nodes continue to scale down, conventional 6-Transistor (6T) SRAM cells suffer from various limitations such as increased leakage currents, degraded stability, and higher susceptibility to read/write failures. These issues are particularly significant in near-threshold voltage operations, where the performance margins become tighter due to reduced supply voltage and process variations.

In low-power applications like Internet-of-Things (IoT), biomedical implants, and wearable electronics, there is a growing need for SRAM architectures that can operate reliably under constrained energy conditions. To overcome the shortcomings of conventional designs, alternative SRAM topologies have been proposed. Among these, the 11-Transistor (11T) SRAM cell offers promising advantages in terms of read/write stability, noise margins, and robustness.

This project presents the design and implementation of a Single-Ended 11T SRAM cell using 18nm FinFET technology, aimed at enhancing read and write operations while minimizing power consumption. The FinFET structure enables superior electrostatic control and reduced leakage compared to planar CMOS devices. An additional NMOS transistor is introduced in the cell structure to separate the read path and prevent half-select disturbances. This not only improves static noise margins but also allows for reliable operation across a wide range of process-voltage-temperature (PVT) variations. The design is validated using simulations in Cadence Spectre, with results showing significant improvements in energy efficiency and performance compared to traditional SRAM cells.

2. IMPLEMENTATION METHODOLOGY

The proposed Single-Ended 11T SRAM cell is implemented using 18nm FinFET technology to leverage its improved leakage control, scalability, and reduced short-channel effects. The 11T structure is developed by modifying the standard 10T SRAM cell, adding an NMOS transistor to isolate the read path and improve both write and read stability. This additional transistor mitigates the half-select issue common in traditional SRAM designs and enhances the noise margins under low-voltage operation.The SRAM cell comprises decoupled read and write paths, allowing the read operation to occur without disturbing the storage node. The write path is carefully designed to overcome write-ability limitations, especially when operating in the near-threshold voltage regime. A single-ended sense amplifier is employed to improve read sensing efficiency with minimal power overhead.Circuit-level simulations are conducted using the Cadence Spectre tool to evaluate critical performance metrics such as Write Static Noise Margin (WSNM), Read Static Noise Margin (RSNM), power consumption, delay, and energy efficiency. The designed 11T SRAM is benchmarked against other variants including 6T, SE10T, ST10T, and conventional 10T SRAM cells. Key blocks such as the sense amplifier and write driver are also designed and verified to ensure compatibility and robustness with the core memory array.Extensive simulations are carried out across multiple corners and conditions, including varying supply voltages and temperatures, to assess the cell's reliability and stability. The architecture demonstrates a favorable trade-off between area, power, and performance, validating its suitability for low-power applications such as embedded processors, IoT nodes, and portable devices.

3. RESULTS: SINGLE-ENDED 11 TRANSISTORS(SE11T) SRAM CELL

3.1 SCHEMATIC DIAGRAM

Table 3.1: Control signals

Control Signal	Write (1)	Write (0)	Hold	Read
WWL	1	1	0	0
WWLA	1	0	0	0
WWLB	1	0	1	1
RWL	0	0	0	1

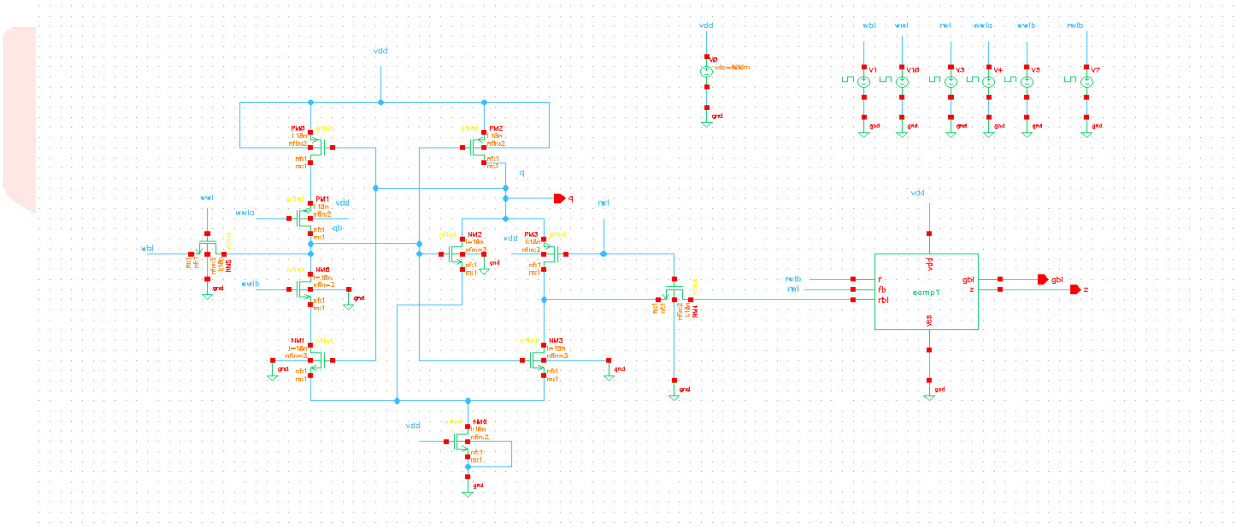

Fig.1 Schematic of SE11T SRAM CELL

3.2 FUNCTIONAL VERIFICATION OF SE11T SRAM CELL:

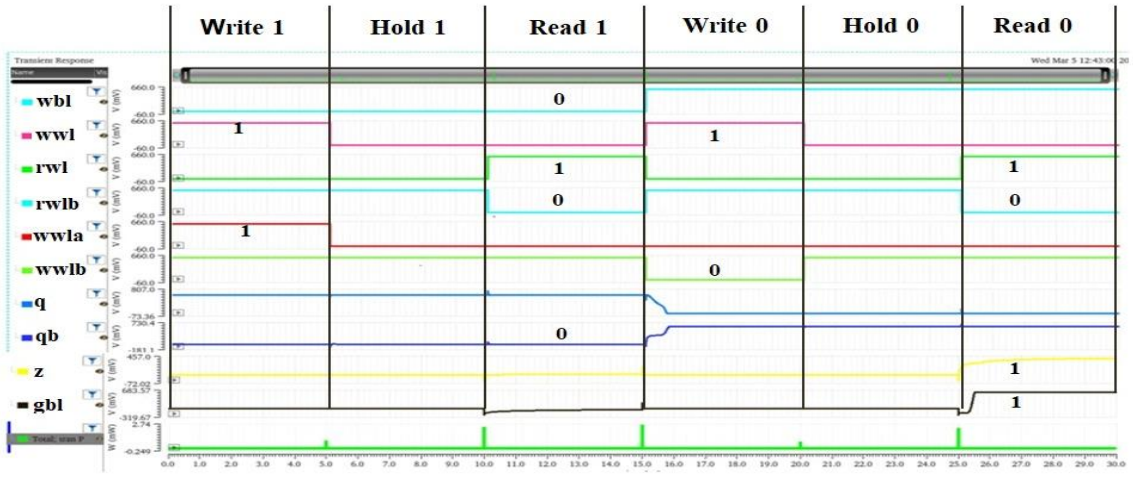

Fig.2 Wave form

3.3 READ AND WRITE STATIC NOISE MARGIN

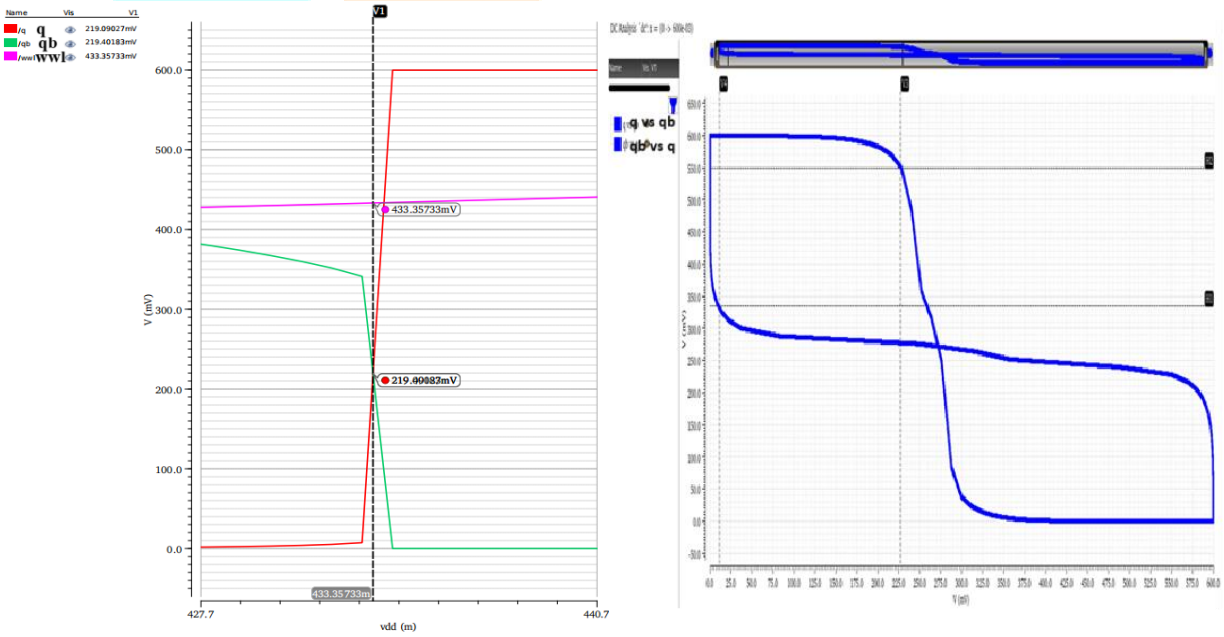

Fig.3 WSNM and RSNM

4. RESULTS AND ANALYSIS

To evaluate the performance and robustness of the proposed modified SE11T SRAM cell, several conventional SRAM cell architectures have been used for comparison. These include the standard 6T SRAM cell, the Static Threshold 10T (ST10T) cell, the standard 10T cell, and the Single-Ended 10T (SE10T) cell. Each of these cells has been implemented and simulated using FinFET technology at the same technology node to ensure consistency. The schematic diagrams of these cells are designed using Cadence Virtuoso and provide a baseline for comparison in terms of stability, power consumption, read/write performance, and area overhead. These standard designs help highlight the advantages and improvements brought by the proposed modified SE11T design, especially in terms of noise margins and enhanced data stability under process variations.

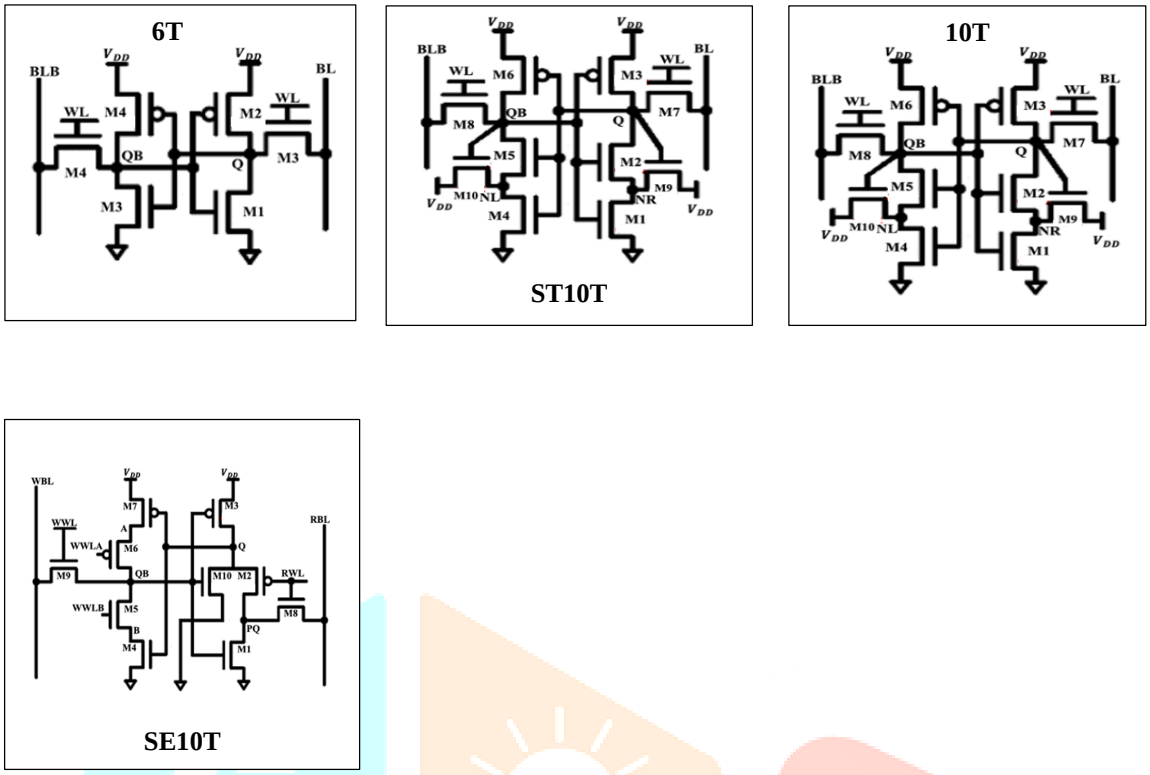

Fig.4 Schematic of the comparison SRAM cells along with transistor sizing

4.1 Output Measures Comparison of Different SRAM Cells

Table 4.1: Comparision table

Parameter	6T	ST10T	10T	SE10T	SE11T
Read delay (ns) at TT/27°C	15.29	15.29	15.06	15.02	15.03
Write delay (ns) at TT/27°C	5.236	5.244	0.03848	0.3691	0.4037
Read Power (µW) at TT/27°C	0.2528	0.2598	5.755	5.745	5.752
Write Power (nW) at TT/27°C	153.1	5923	42.32	34.7	41.27
Read Energy (fJ) at TT/27°C	7.805	7.906	172.6	172.3	172.6
Write Energy (fJ) at TT/27°C	4.59	177.7	1.27	1.041	1.238
Write SNM (mV) at TT/27°C	66	96	76	164	166
Leakage Power (µW) at TT/27°C	0.013490	0.013633	6.7792	0.007233	6.7832
Read SNM (mV) at TT/27°C	200	206	207	210	216

As shown in Table 1, the Single-Ended 11T SRAM Cell is designed to improve both write and read stability compared to traditional SRAM architectures. The simulation results clearly indicate that the SE11T cell achieves lower read and write delay, which contributes to high-speed performance. Additionally, it offers the highest Read Static Noise Margin (RSNM) and Write Static Noise Margin (WSNM), confirming its robustness during read/write operations.

However, this improvement comes at the cost of increased leakage power, as the additional NMOS transistor in the SE11T design remains constantly ON. Despite this, the enhanced stability and speed make it a superior choice for low-power, energy-efficient applications, particularly in domains like portable electronics, IoT systems, and embedded memory designs.

4.2 ANALYSIS

CORNER ANALYSIS: Corner analysis is a method used in semiconductor circuit design to evaluate the performance of a circuit under different process, voltage, and temperature (PVT) variations.

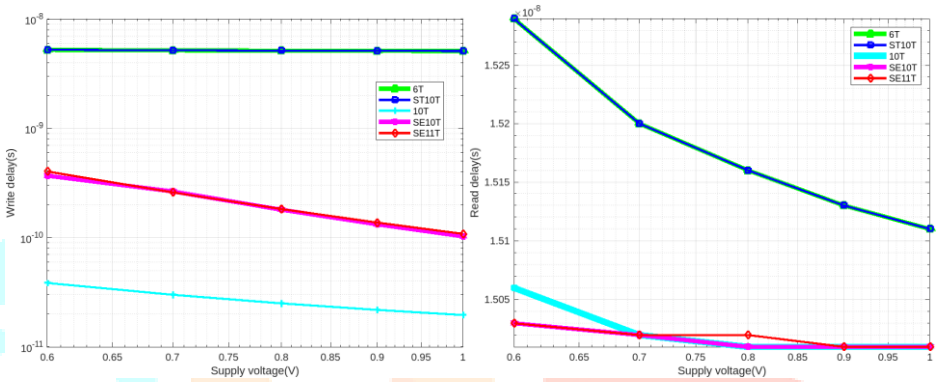

Fig.5 Write delay and Read delay of different SRAM cells

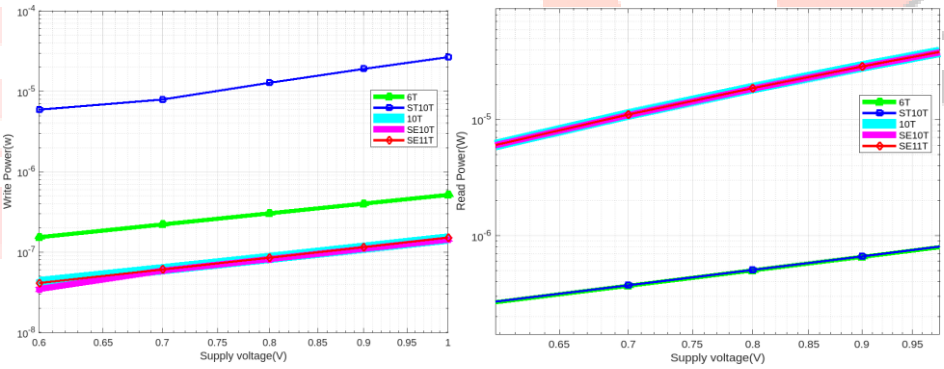

Fig.6 Write power and Read power of different SRAM cells

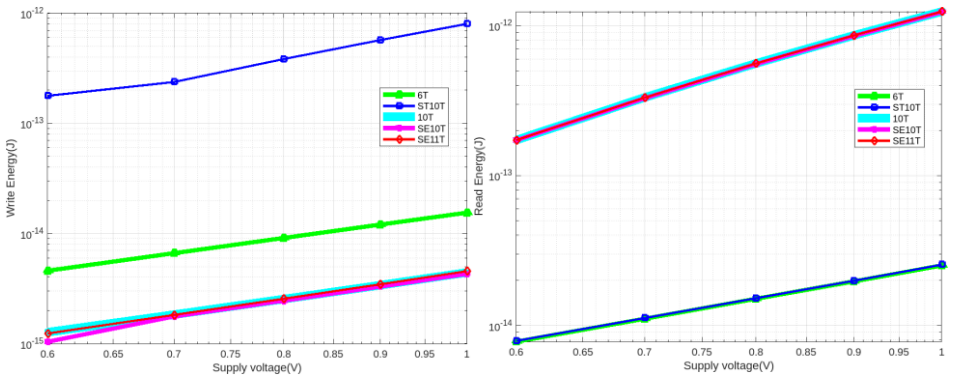

Fig.7 Write energy and Read energy of different SRAM cells

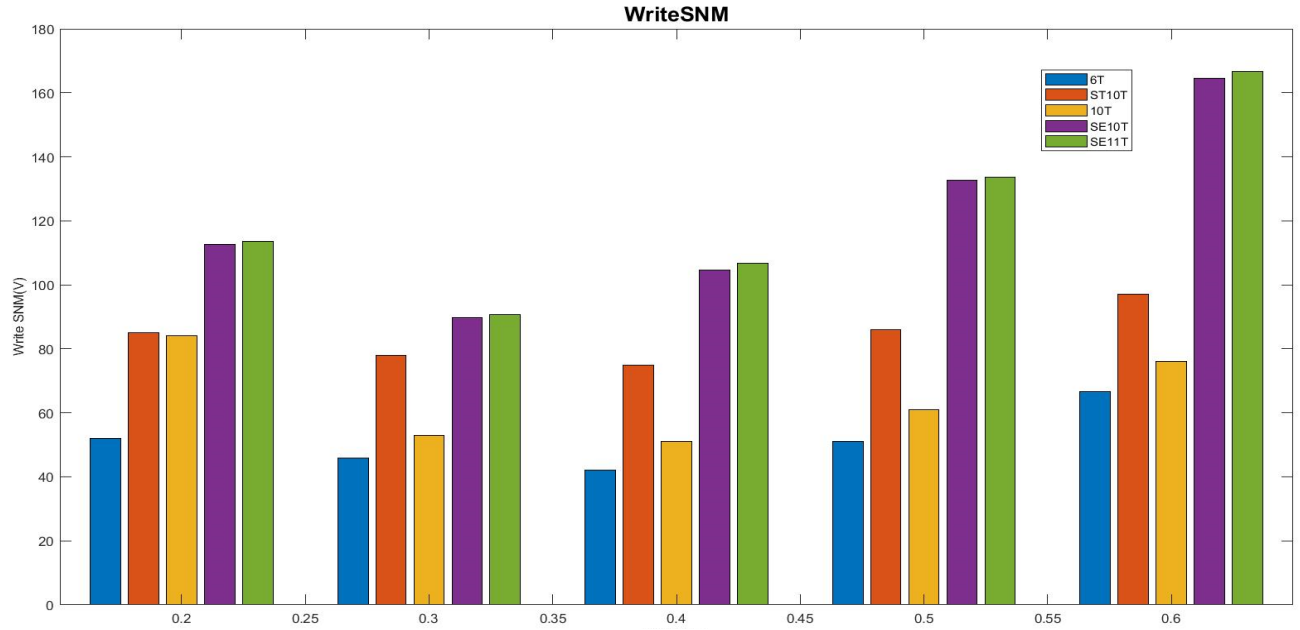

Fig.8 Write Stability Comparison of SRAM Cells at various Voltages

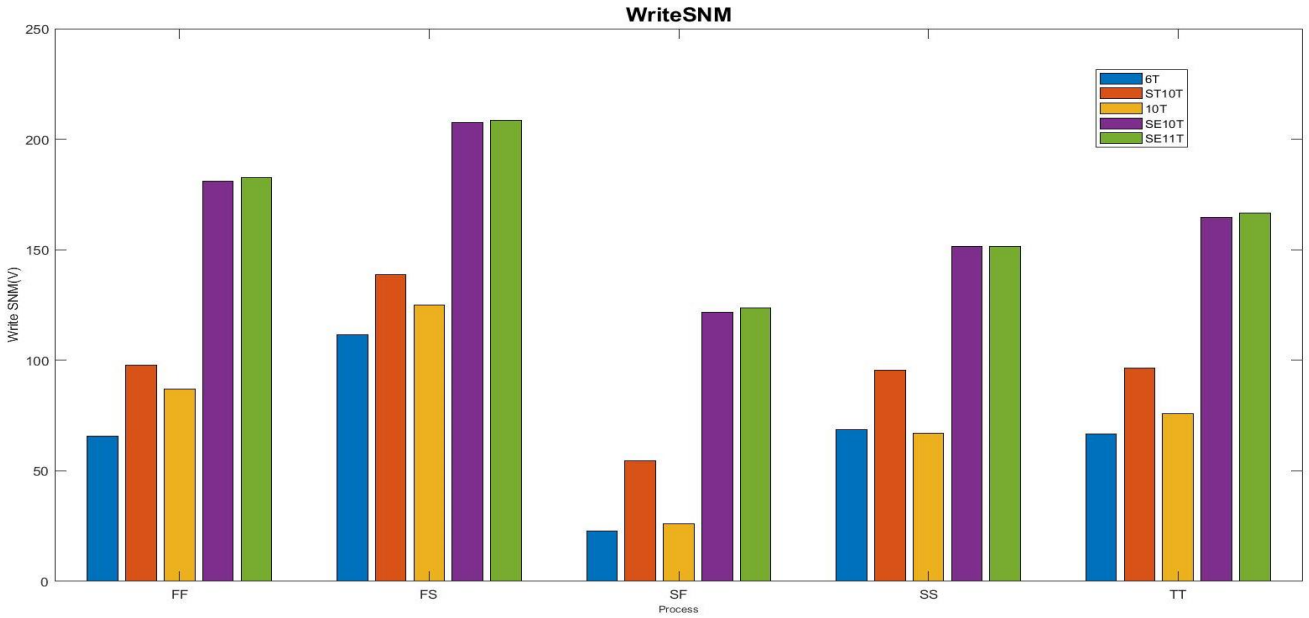

Fig.9 Write Stability Comparison of SRAM Cells at various Processes

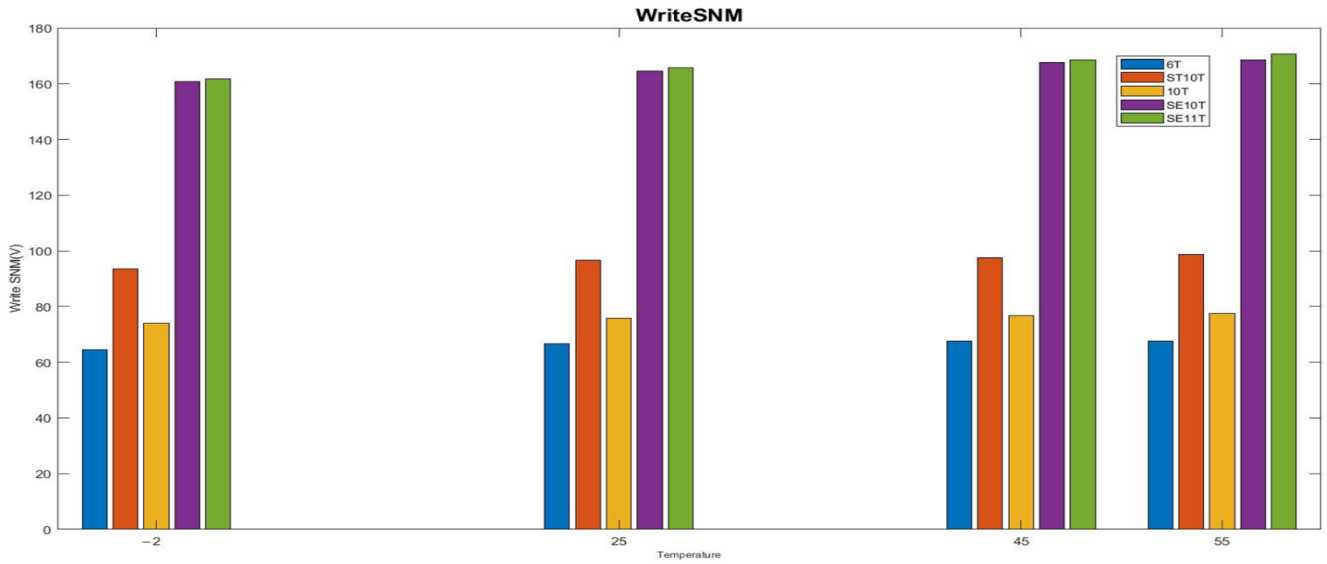

Fig.10 Write Stability Comparison of SRAM Cells at various Temperatures

5. CONCLUSION

In this project, the write stability of a Single-ended 10T SRAM Cell is improved by incorporating an additional transistor, thus transforming it into an Single-ended 11T SRAM Cell. The modification effectively addressed write stability issues by optimizing the write margin. The additional transistor provided better control over write operations without significantly impacting read performance or power consumption. The performance of the circuit has been evaluated under various voltages, processes and temperatures and the write stability has been improved compared to other SRAM Cells. The read stability of the Single-ended 11T SRAM Cell has also been improved. This improvement is particularly beneficial for low-power and high-performance memory applications, where reliability and efficiency are critical.

REFERENCES

[1] E. Abbasian and S. Sofimowloodi, "Energy-Efficient Single-Ended Read/Write 10T Near Threshold SRAM," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 70, no. 5, pp. 2037-2047, May 2023, doi: 10.1109/TCSI.2023.3247807.

[2] Shourya Gupta, Kirti Gupta, Benton H. Calhoun and Neeta Pandey "Low-Power Near Threshold 10T SRAM Bit Cells With Enhanced Data-Independent Read Port Leakage for Array Augmentation in 32-nm CMOS," in IEEE Transactions on Circuits And Systems–I: Regular Papers, Vol. 66, No. 3, March 2019.

[3] Yajuan He, Jiubai Zhang, Xiaoqing Wu, Xin Si and Bo Zhang, "A Half-Select Disturb-Free 11T SRAM Cell With Built-In Write/Read-Assist Scheme for Ultralow-Voltage Operations", in IEEE Transactions on Very Large Scale Integration (Vlsi) Systems, Vol. 27, No. 10, October 2019.

[4] Jebamalar Leavline, Sugantha A. "An efficient common source sense amplifier for single ended SRAM", in ELSEVIER on Memories-Materials, Devices, Circuits and Systems 5 2023.

[5] Vyshna P and Dr.Jinsa Kuruvilla, "Design Of Sense Amplifier For Sram With Low Power Consumption And High Stability", in International Journal for Research in Engineering Application & Management (IJREAM) ISSN : 2454-9150 Vol-05, Issue-03, June 2019.

[6] Ravi Hosamani, Anusha Kalasur and Anusha Bhat " Design and Analysis of 1-Bit SRAM", in International Journal of Engineering Research & Technology (IJERT) ISSN: 2278-0181 Vol. 9 Issue 09, September-2020.

[7] Saloni Bansal and V.K.Tomar "10T SRAM cell Analysis for improved Read and Write Noise Margin", in IEEE Transactions on Circuits and Systems 2023

[8] Sayeed Ahmad, Mohit Kumar Gupta, Naushad Alam and Mohd.Hasan " Single-Ended Schmitt-Trigger-Based Robust Low-Power SRAM Cell" , IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 24, No. 8, August 2016

[9] Juhyun Park, Younghwi Yang, Hanwool Joeng, Seung Chul Song, Joseph Wang, Geoffrey Yeap and Seong-Ook Jung "Design of a 22-nm FinFET-Based SRAM With Read Buffer for Near-Threshold Voltage Operation", IEEE Transactions On Electron Devices, Vol. 62, No. 6, June 2015