IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

Implementation Of Exclusive OR Gate Using Dynamic Pass Transistor Logic With Low Latency

[1]S Jayachandranath, [2]K Seshidar ,[3]I C Narasimha ,[4]T Hussaini, [5]C Nagendra Reddy
[1,2,3,5] Assistant Professor, [4,]Associate Professor,
Department of ECE
[1,2,5]SVR Engineering College, Nandyal, [3]Tadipatri Engineering College, Tadipatri, [4,]Viswam Engineering College, Madanapalle

Abstract: Dynamic Pass transistor logic used in the digital circuits to reduce the transistor count, it arises node to get discharged properly, even with the pull-down network OFF during evaluation. An EXOR gate is implemented with the dynamic logic where clock signal is directly accessed the stacking effect circuitry, and it is altered to implement a new design of static CMOS dynamic logic with lower leakage power than older designs that used in nano meter technology the Micro wind 10nm technology used to validate the logic design methods and implementation of pass transistor logic with low input logic

***Index Terms*- Ex-OR, Dynamic logic, Pass Transistor Logic**

1. Introduction

In today's VLSI circuit design, high performance and low power consumption have become crucial.Re search efforts in the field of low power VLSI systems have increased in tandem with the exponential grow th of portable electronic devices such as laptops, multimedia devices, and cellular handsets.These days, on e of the most crucial design factors for IC designers is low power consumption along with minimal delay a nd space requirements.

In VLSI circuits, power consumption mostly comes from three sources There is more design flexibility for hybrid CMOS logic designs to get the required performance. A hybrid full adder is faster, uses less power, and performs better[3]. In many circuits that execute arithmetic operations including addition, subtraction, multiplication, address computation, comparator, and MAC, among others, full adders are essential components. Improving the full adders' performance has a big impact on the system's overall performance.

When developing a complete adder, there are two logical approaches: static style and dynamic styl e.While dynamic full adders are faster and occasionally more compact than static ones, static full adders ar e more dependable, straightforward, and require less power.Techniques for achieving power consumption at the expense of performance are provided by recent technological scaling and the usage of several logic f amilies.ower, speed, and durability are so important to cuttingedge designs that they must be considered at every stage of the design process.[2]

At the circuit level, the selection of logic styles is a crucial limitation.the energy, delay, area, and r obustness of logic types vary.In order to satisfy each circuit requirementdesigners must select circuits from various locations on an energy delayrobustness envelope because every design necessitates tradeoffs and compromises.Future computing need a logic style that satisfies several requirements, including high perfor mance, low power consumption, great robustness against noise and variability, and ease of implementation and testing.[2]

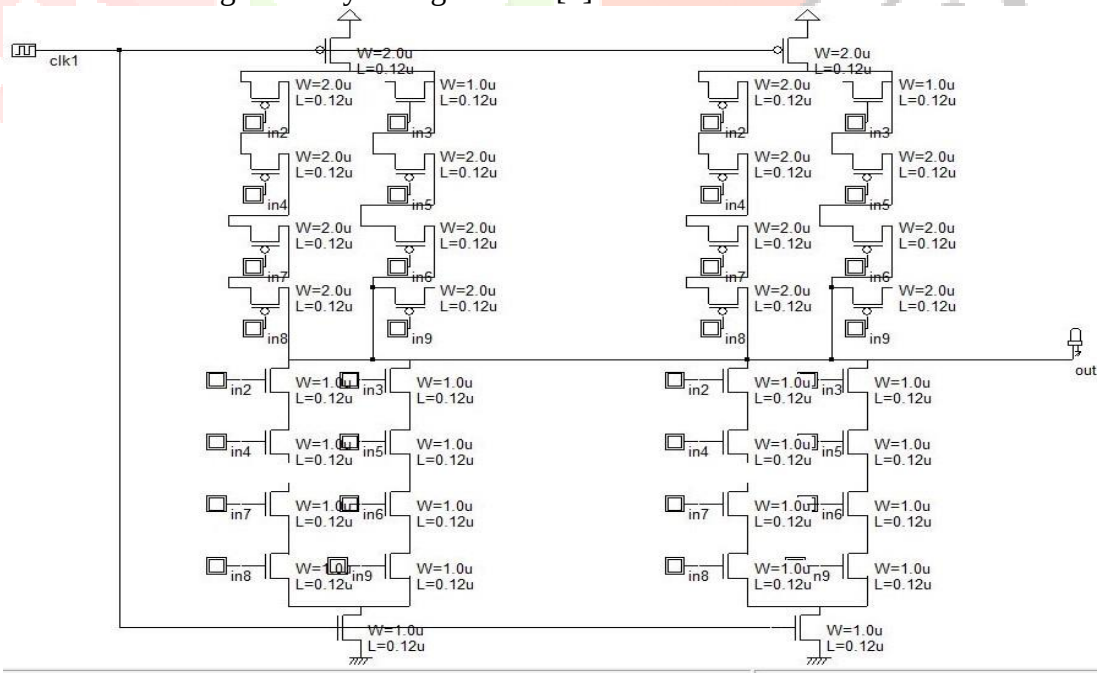
To further increase resilience, we also wish to employ logic styles that work with various kinds of logi c implementation.The goal of this research project is to adapt and enhance dynamiclogic logic in order to s ignificantly enhance performance, speed, area overhead, and power usage. Since Dynamic pass transistor p- type logic is a timed logic family, there is a clock signal present in each logic. Node N0 becomes high when the clock signal becomes low, which lowers the gate's output. the process by which the gate output is driven low after being driven high. [6]The recharge phase is the time a cell operates when both its input and output are low. The evaluate phase is the following stage, which occurs when the clock is high.

2. Dynamic PT with EX-or gates.

Dynamic pass transistor logic implementation along with pass transistor logic where For the SPICE simulations to be accurate, we took great pains to optimize the process file for all ranges of operation. This optimization was accomplished using dynamic pass transistor logic with that software, we measured isolated bulk transistors and extracted the optimized process file. The transistors were made using a 0. 18- m process with a 0. 3 - V. the resulting process files were used in SPICE circuit simulations for power and delay measurements over various supply voltages and loads. Each transistor was decomposed into ten transistors that contain 1/10 desired width to provide accuracy for the RC delay associated with charging the body

As mentioned earlier, traditional scaling analyses emphasize the importance of trying to maintain a constant to preserve the switching speed [2]. As we try to scale below 1 V,it becomes tempting to raise this ratio slightly. Unfortunately, this is not the only source of delay penalty when we raise the ratio. In single-transistor pass-gate logic, a drop is lost across the device when it tries to pull the output high [3], [5], [8], [9], [11], [13], [14]. This signal degradation subsequently slows the pulldown of the output buffer and causes leakage because the pullup is not fully off. Since DTMOS circuits potentially lower the on-state threshold voltage to zero or below [15], pass-gate logic may benefit further from such designs.

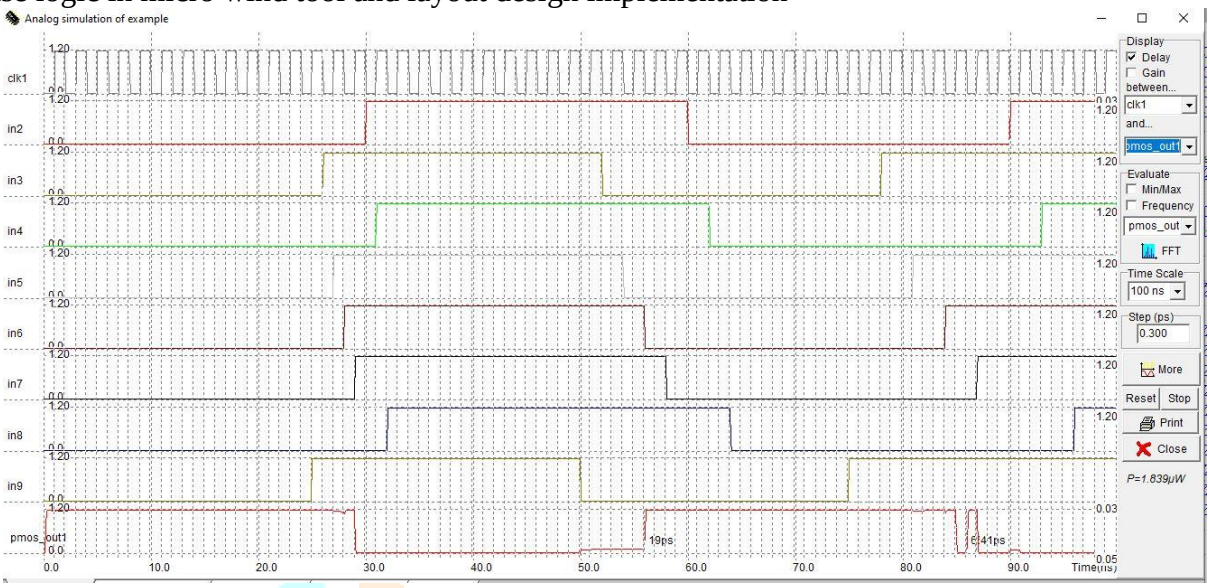
In dynamic logic cells, the evaluate phase is the functional functioning phase, and the recharge phase makes it possible for the evaluate to phase to take place.The critical path in dynamic pass transistor logic cells that develops high efficiency on the adder and other applicationthat passes through cells in the evaluate phase tanks to the clock signal's application.No pullup PMOS transistors need to be driven by the inputs because the dynamiclogic cell only shifts from a low to a high direction.Because there is not a PMOS transistor, the effective transistor width loads down a prior logic stage, dynamiclogic over static logic for a given current drive.This is crucial because the high speed guarantees that a speed advantage can be obtained without significantly taxing the cell.[6]



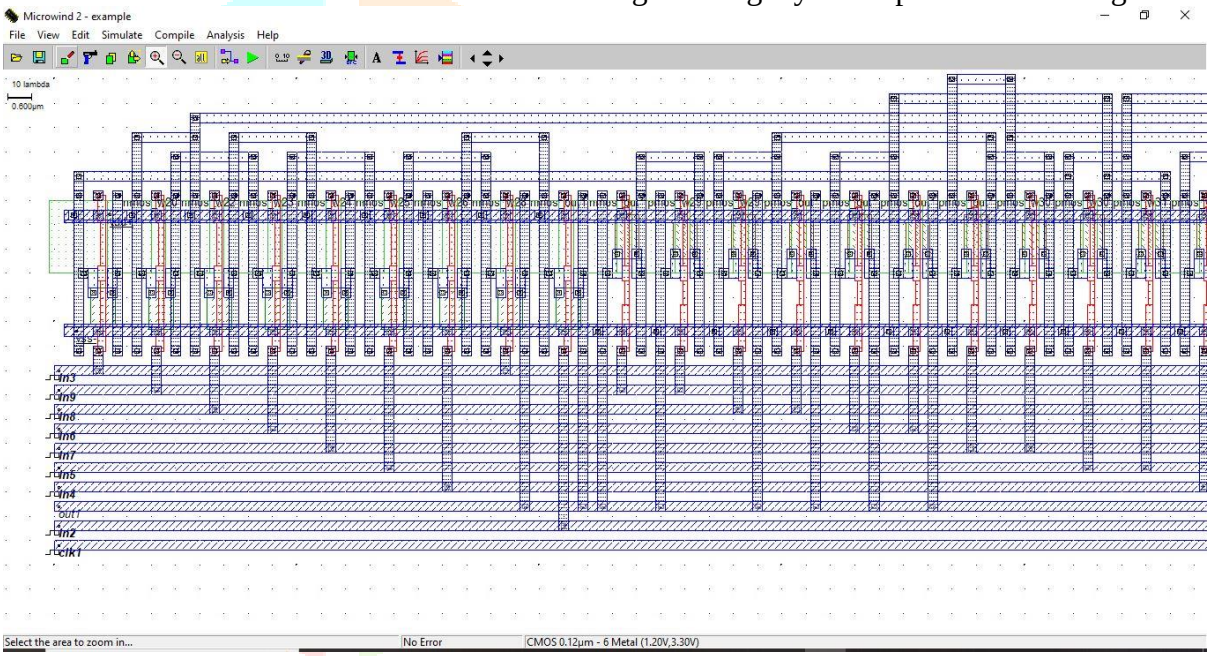
Design of Dynamic Pass transistor logic Exclusive OR gate

3. Results

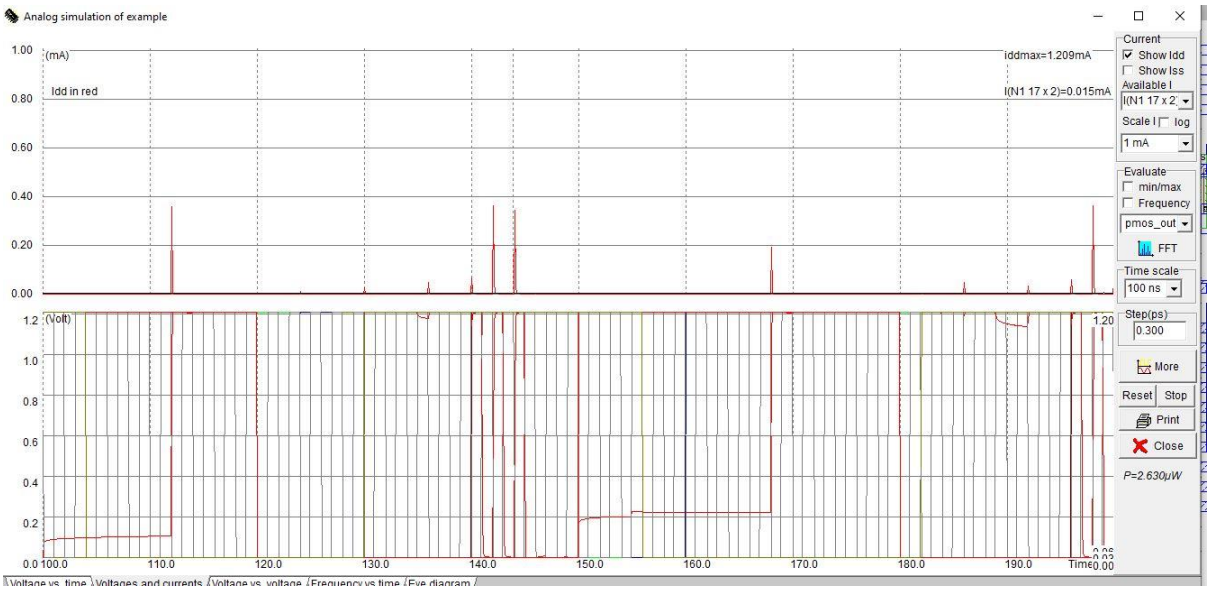
The results and discission on dynamic pass transistor logic during pre-charge phase and evaluation phase logic in micro wind tool and layout design implementation



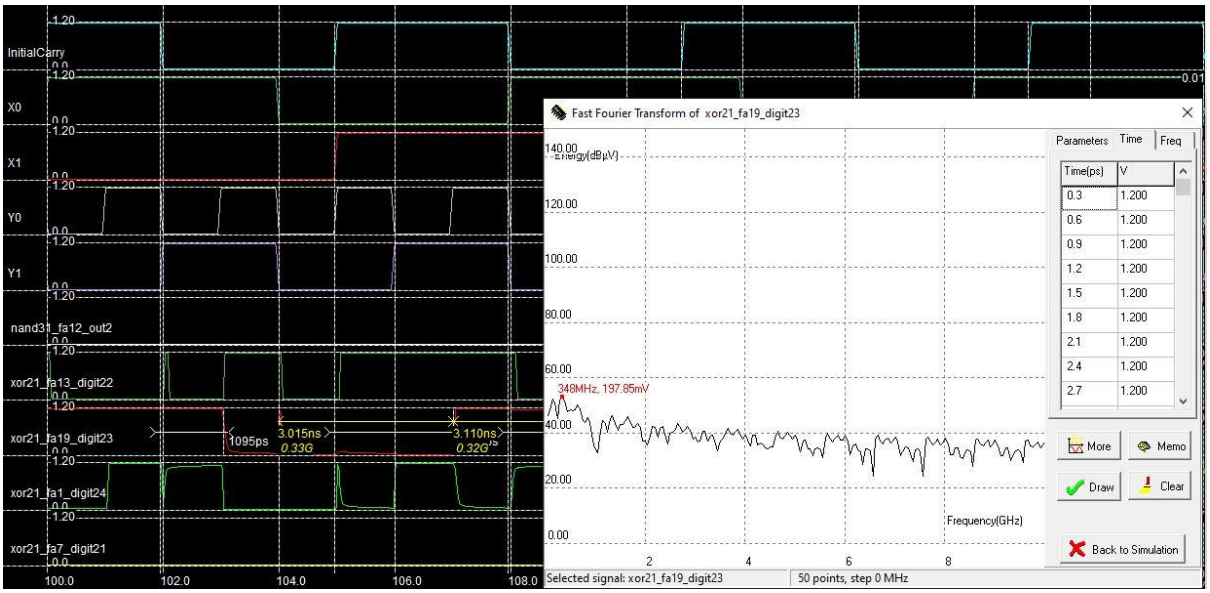
Simulation results for Exclusive or gate using Dynamic pass transistor logic



Layout Design of implementation results for Exclusive or gate using Dynamic pass transistor logic



Simulation results for Exclusive or gate using Dynamic pass transistor logic



Simulation results for Exclusive or gate using Dynamic pass transistor logic

References

[1] B. Parhami, Computer Arithmetic, Algorithm and Hardware Design, *Oxford University Press,* New York, pp. 91-119, 2000.

[2] Stephen Brown and Zvonko Vranesic, Fundamentals of Digital Logic with VHDL Design. *2nd Ed. McGraw-Hill Higher Education,* USA.ISBN: 0072499389, 2005.

[3] B. Goll and H. Zimmermann, "A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65," *IEEE Trans. Circuits Syst. II, Exp. Briefs,* vol. 56, no. 11, pp. 810–814, Nov. 2009.

[4] Jinhui Wang, Wuchen Wu, Ligang Hou, Shuqin Geng and Wang Zhang, Xiaohong Peng, "Using Charge Self-compensation Domino Full-adder with Multiple Supply and Dual Thresho

[5] M. S. Abadir and H. K. Reghabati, "Functional test generation for digital circuits described using binary decision diagram," *IEEE Trans. Comput.*, vol. C-35, pp. 375–379, Apr. 1986.

[6] S. B. Akers, "Binary decision diagrams," *IEEE Trans. Comput.*, vol.C-27, pp. 509–516, June 1978.

[7] W. Al-assadi, A. P. Jayasumana, and Y. K. Malaiya, "Pass-transistor logic design," *Int. J. Electron.*, vol. 70, pp. 739–749, 1991.

[8] P. Ashar, S. Devadas, and K. Keutzer, "Testability properties of multilevel logic networks derived from binary decision diagrams," in *Proc.Santa Cruz Conf. Advanced Res. VLSI*, Mar. 1991, pp. 35–54.

[9] C. L. Berman, "Ordered binary decision diagrams and circuit structures,"in *Proc. IEEE Int. Conf. Computer Design: VLSI in Computers,* 1989, pp. 392–395.

[10] K. Bartlett, R. K. Brayton, G. Hachtel, R. Jacoby, R. Rudell, A. Sangiovanni-Vincentelli, and A. Wang, "Multilevel logic minimization using implicit don't cares," *IEEE Trans. Computer-Aided Design*, vol.7, pp. 723–740, 1988.

[11] J. R. Burch, E. M. Clarke, K. L. McMillan, and D. L. Dill, "Sequential circuit verification using symbolic model checking," in *Proc. 27thIEEE/ACM Design Automat. Conf.*, 1990, pp. 46–51.

[12] S. Chakravarty, "A testable multiplexer realization of CMOS combination circuits," in *Proc. 1989 IEEE Int. Test Conf.*, pp. 509–518.

[13] S. Chakravarty, "A characterization of binary decision diagrams," *IEEETrans. Comput.*, vol. 42, pp. 129–136, Feb. 1993.

[14] T. S. Cheung and K. Asada, "Regenerative pass-transistor logic: A circuit technique for high speed digital design," *IEICE Trans. Electron.*,vol. E79-C, no. 9, pp. 1274–1284, Sept. 1996.

[15] A. Jaekel, "Synthesis of multilevel pass transistor logic networks," Ph.D. dissertation, University of Windsor, 1995.

[16] G. A. Jullien, W. C. Miller, R. Grondin, L. Del Pup, S. Bizzan, and D.Zhang, "Dynamic computational blocks for bit-level systolic arrays," *IEEE J. Solid-State Circuits,* vol. 29, no. 1, pp. 14–22, 1994.

[17] G. A. Jullien, N. M. Wigley, and J. Reilly, "VLSI implementations of number theoretic concepts with applications in signal processing," invited chapter in *Handbook of Statistics*, N. K Bose and C. R. Rao Eds. Elsevier Science Publishers, 1993, vol. 10, ch. 13, pp. 535–576.

[18] Y. Kanie, Y. Kubota, S. Toyoyama, Y. Iwase, and S. Tsuchimoto, "4-2 compressor with complementary pass-transistor logic," *IEICE Trans.Electron.*, vol. E77-C, no. 4, pp. 647–649, Apr. 1994