



Multilevel Inverter Topologies with Reduced Number Switches by Using Selective harmonic elimination technique

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Abstract: Techniques like selective harmonic reduction are proposed in this project's proposal. The harmonic content of a single phase cascaded multilevel inverter was reduced using SHE. For inverters with five to eleven levels of levels, the firing instants for the electronic switches are computed off-line. Four independent voltage sources with voltage output levels in a certain ratio make up the novel module structure proposed in this concept. In recent years, multilevel inverters have been a hot topic because of their ability to handle high-power applications. This paper suggests. To minimise harmonic content in a single-phase cascaded multilevel inverter, this study uses the selective harmonic elimination approach. As output levels grow, so does the number of switching components required to perform the switch. There is a risk of power loss and a decrease in overall system efficiency due to the increased number of switches. Most notable is that the module may be utilised as a submultiple level structure and expanded for any number of levels with minimum increase in switching components (pho). MLI's superior power quality, decreased total harmonic distortion (THD), lower voltage stress across the switches, improved electromagnetic compatibility, and fewer switching losses are attracting a lot of attention.

Keywords: Selective harmonic elimination technique, Total harmonic distortion (THD), multilevel inverter (MLI)

I. INTRODUCTION

For many years, industries have relied on induction motor drives to provide precise control over speed. This is due to the induction motor's simple design and low maintenance requirements. For induction motor driving applications, multilayer inverters (MLI) are becoming more common [1-3]. Medium to high-voltage and high-current driving applications call for it in particular. Multilevel inverters provide several benefits over regular inverters. THD, switching losses, power quality, and decreased electromagnetic interference are the main benefits (EMI). Reduced voltage stress on each component is the primary benefit of a multilayer inverter [4-8]. Multilevel inverter topologies may be broken down into three sorts. They are flying capacitor, diode clamped, and H-bridge cascaded multi-level inverters. "

For medium voltage (MV) drives, the most common inverter architecture is the H-bridge multilevel inverter. Single-phase H-bridge power cells make up the majority of the structure. In reality, the number of power cells in an H-Bridge inverter is controlled mostly by its operating voltage and manufacturing costs. For the same voltage level, the H-bridge multilevel inverter needs fewer components than any other form of inverter [9-11]. Various modulation strategies were developed as a result of the evolution of multilayer inverters [12]. Locomotive and track-side static converters [13] have been the most popular places to first see multilevel converters put to use. Active filtering, high-voltage motor control, high-voltage direct current (dc) transmission and, most recently, formedium voltage induction motor variable speed drives [12-15] are some of the most recent uses for power system converters. Flexible AC Transmission System (FACTS) and industrial medium-voltage motor drives are only a few of the many multilayer converter uses. As a result, multilayer inverters have become more popular in industrial applications, such as motor drives, static VAR compensators, and renewable energy systems. The stepwise output voltage of multilayer inverters is a big benefit over standard two-level voltage source inverters. A three-phase MLI design with the fewest switches is shown in this study. This research presents a novel multilayer inverter architecture with fewer switches than typical MLIs to alleviate the drawbacks.

II. SELECTIVE HARMONIC ELIMINATION

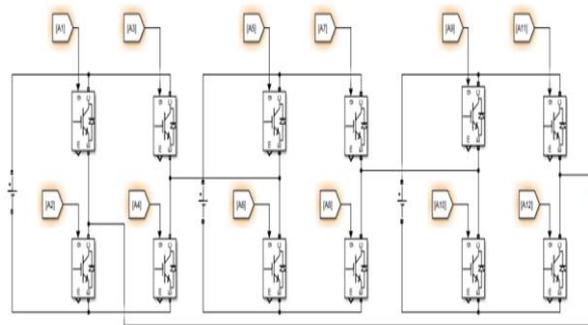
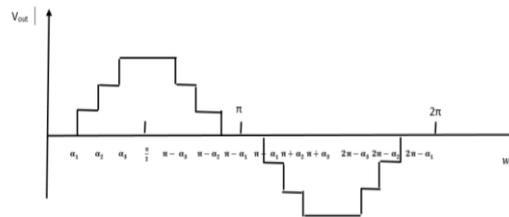
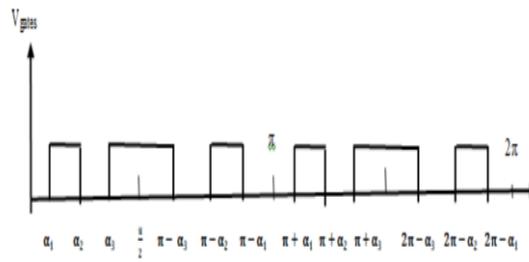
In this method, the number of harmonics to be removed is determined. Harmonics from the 3rd and 5th levels of a seven-level inverter, for example, must be removed. Figure 1 depicts an off-line determination of the multilevel inverter's switching instants. A mirror copy of 2 is created around the figure's 1 and 2 points, which is what we require for the inverter's positive cycle output. Then, the process repeats itself for the next cycle, which is negative. Figure 3.2 shows the estimated output voltage for each MOSFET switch based on these instants. Using a seven-level MLI, the MOSFET switches' states, periods of operation, and levels of output voltage are summarised in Table 3.1 and Figure 3.3. To get the triggering angles 1, 2, and 3, we must solve the nonlinear equation shown below.

$$1 - \cos\alpha_1 + \cos\alpha_2 - \cos\alpha_3 = \frac{4V_s}{\pi}$$

$$1 - \cos3\alpha_1 + \cos3\alpha_2 - \cos3\alpha_3 = 0$$

$$1 - \cos5\alpha_1 + \cos5\alpha_2 - \cos5\alpha_3 = 0$$

A Newton Raphson method is used as a common numerical solver for nonlinear solution, which determines the values to be: $\alpha_1 = 13.22^\circ$, $\alpha_2 = 38^\circ$ and $\alpha_3 = 82.9^\circ$.



S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	Period	DC level
1	0	1	0	1	0	1	0	1	0	1	0	α_1	0
1	1	0	0	1	0	1	0	1	0	1	0	$\alpha_2 - \alpha_1$	$+V_{DC}$
1	1	0	0	1	1	0	0	1	0	1	0	$\alpha_3 - \alpha_2$	$+2V_{DC}$
1	1	0	0	1	1	0	0	1	1	0	0	$\pi - 2\alpha_3$	$+3V_{DC}$
1	1	0	0	1	1	0	0	0	1	0	1	$\alpha_3 - \alpha_2$	$+2V_{DC}$
1	1	0	0	0	1	0	1	0	1	0	1	$\alpha_2 - \alpha_1$	$+V_{DC}$
0	1	0	1	0	1	0	1	0	1	0	1	$2\alpha_1$	0
0	0	1	1	0	1	0	1	0	1	0	1	$\alpha_2 - \alpha_1$	$-V_{DC}$
0	0	1	1	0	0	1	1	0	1	0	1	$\alpha_3 - \alpha_2$	$-2V_{DC}$
0	0	1	1	0	0	1	1	0	0	1	1	$\pi - 2\alpha_3$	$-3V_{DC}$
0	0	1	1	0	0	1	1	1	0	1	0	$\alpha_3 - \alpha_2$	$-2V_{DC}$
0	0	1	1	1	0	1	0	1	0	1	0	$\alpha_2 - \alpha_1$	$-V_{DC}$
1	0	1	0	1	0	1	0	1	0	1	0	α_1	0

III. IMPLEMENTATION OF MULTILEVEL SINGLE-PHASE INVERTER

To create voltage harmonics, ErsoyBaser offers a single-phase multilevel inverter. Using a PIC18F45 microprocessor, the switching signals are generated. An inverter with three H-bridge components may provide up to 14 levels of output voltage, according to Tapan Kumar's modelling and actual implementation. Arduino boards based on the ATmega 2560 microcontroller [9] are used to create MOSFET set signals. Using an SPWM cascaded full bridge single phase 7-level inverter, PouyaTarassadi and colleagues [10] present an improved shift modulation inverter. Cascaded multilayer inverter implementation for endless layers is the focus of this study.. The controller receives an off-line programme for each level of the cascaded MLI, and the corresponding triggering events are sent to the MOSFETs. It is contrasted to a Simulink model created specifically for this purpose. A single-phase multilevel inverter with cascaded three H-bridge units [11]-[17] may generate any multilayer output voltage. Improved use of dc power supply and lower harmonic distortion may be achieved using a new multi-level singlephase inverter adopting vector control. [18-20]. In cascaded H bridge inverters, low switching frequency management minimises power losses while increasing the THD factor [21]-[27].

IV. SIMULATION RESULTS:

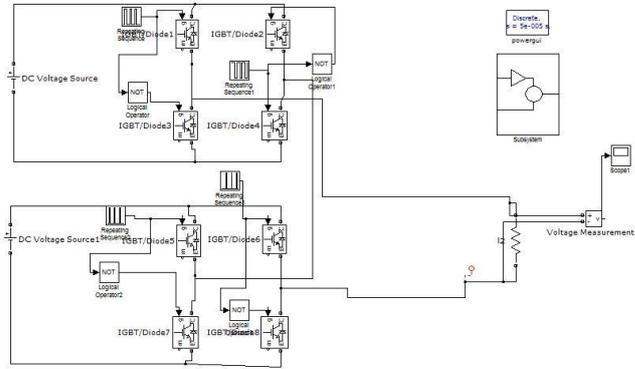


Fig 4 Simulink Diagram of Five level MLI with without PWM Technique

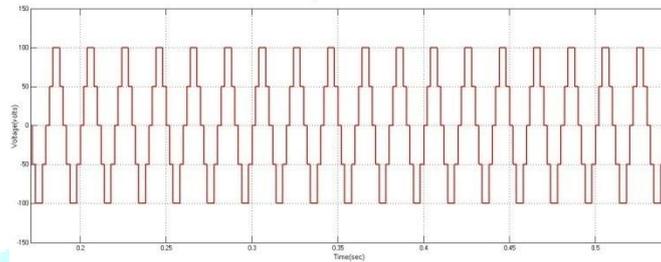
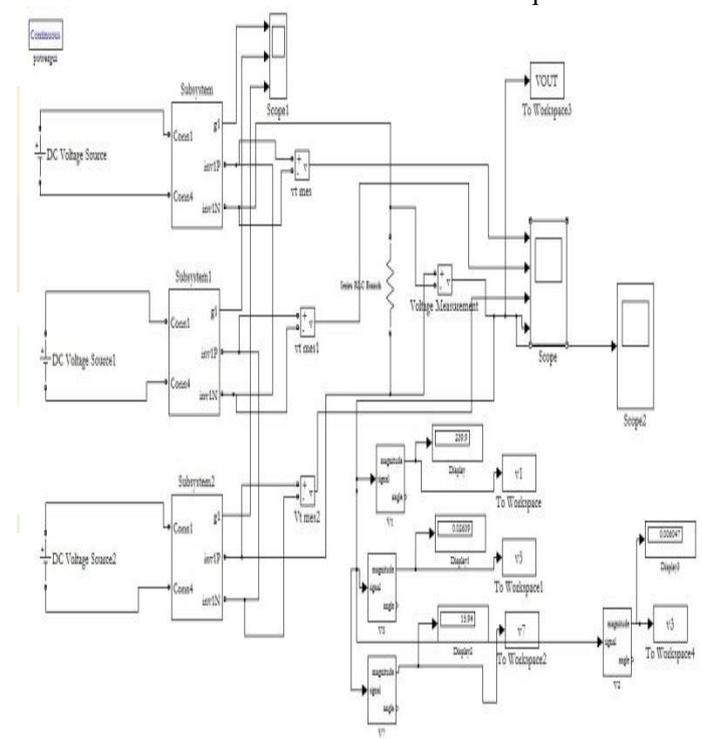
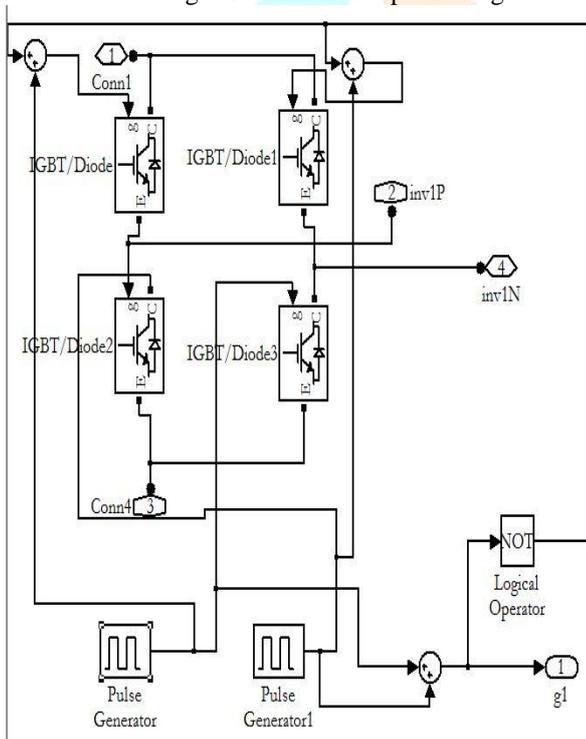


Fig 5 Simulation Output Voltage waveform of five levels MLI with without PWM Technique



(a)

(b)

Fig 6 Simulink Diagram of Seven levels MLI with Selective harmonic elimination technique (SHE) PWM Technique

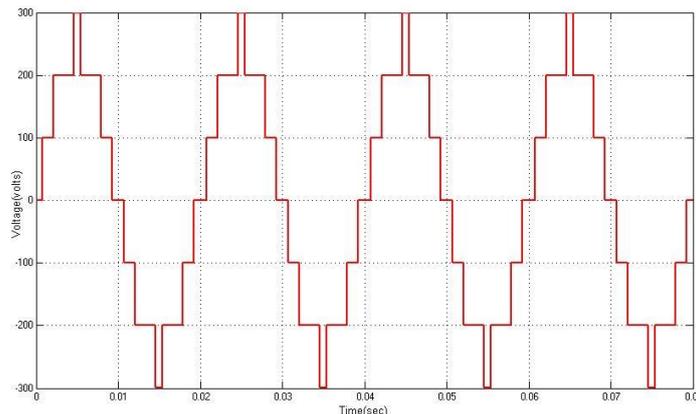


Fig 7 Simulation output voltage waveform of seven levels MLI with Selective harmonic elimination technique (SHE) PWM Technique

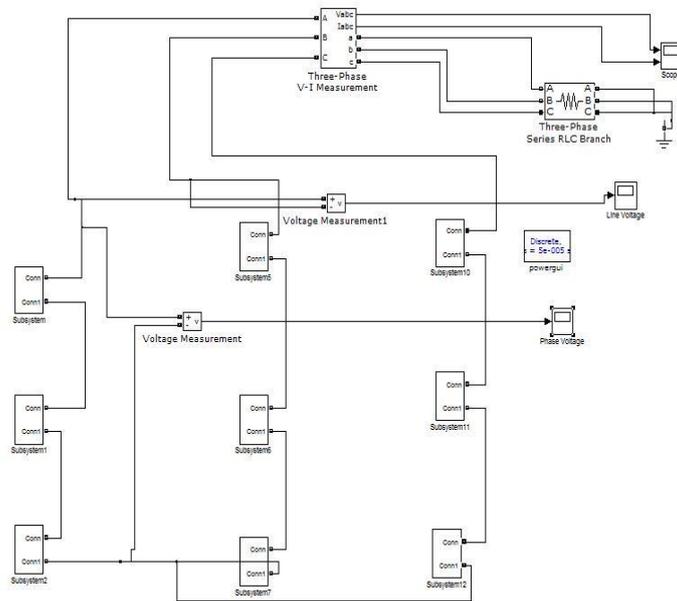


Fig 8 Simulink Diagram of Seven levels MLI with PWM Technique

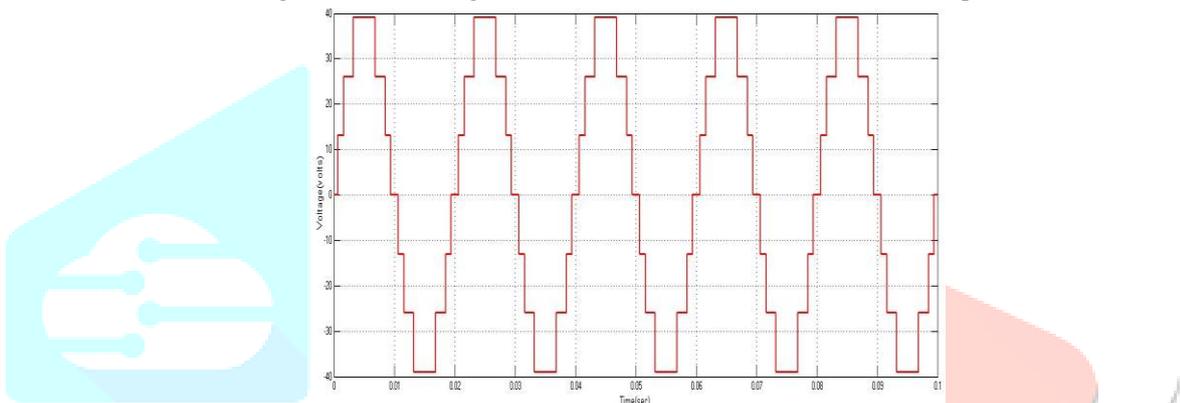


Fig 9 Simulation output voltage waveform of seven levels MLI PWM Technique

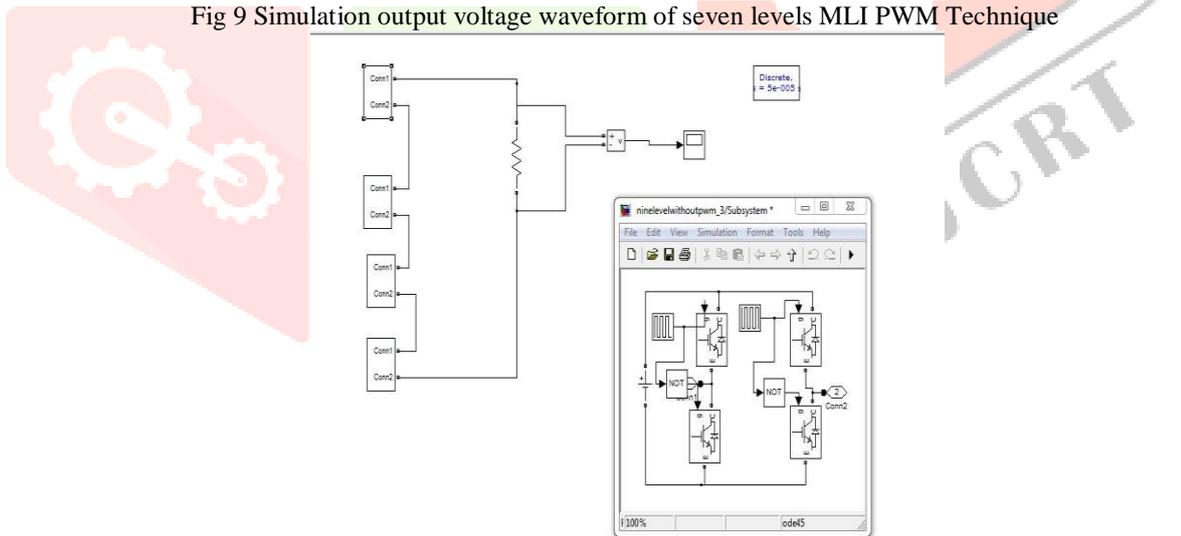


Fig 10 Simulink Diagram of Nine levels MLI without PWM Technique

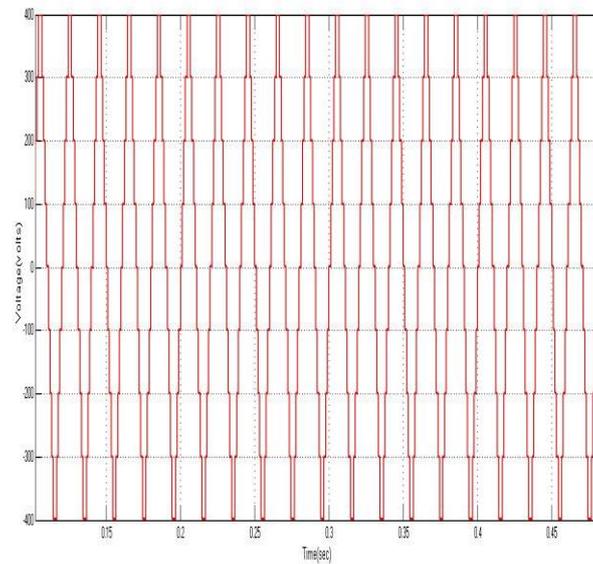


Fig 11 Simulation output voltage waveform of nine levels MLI without PWM Technique

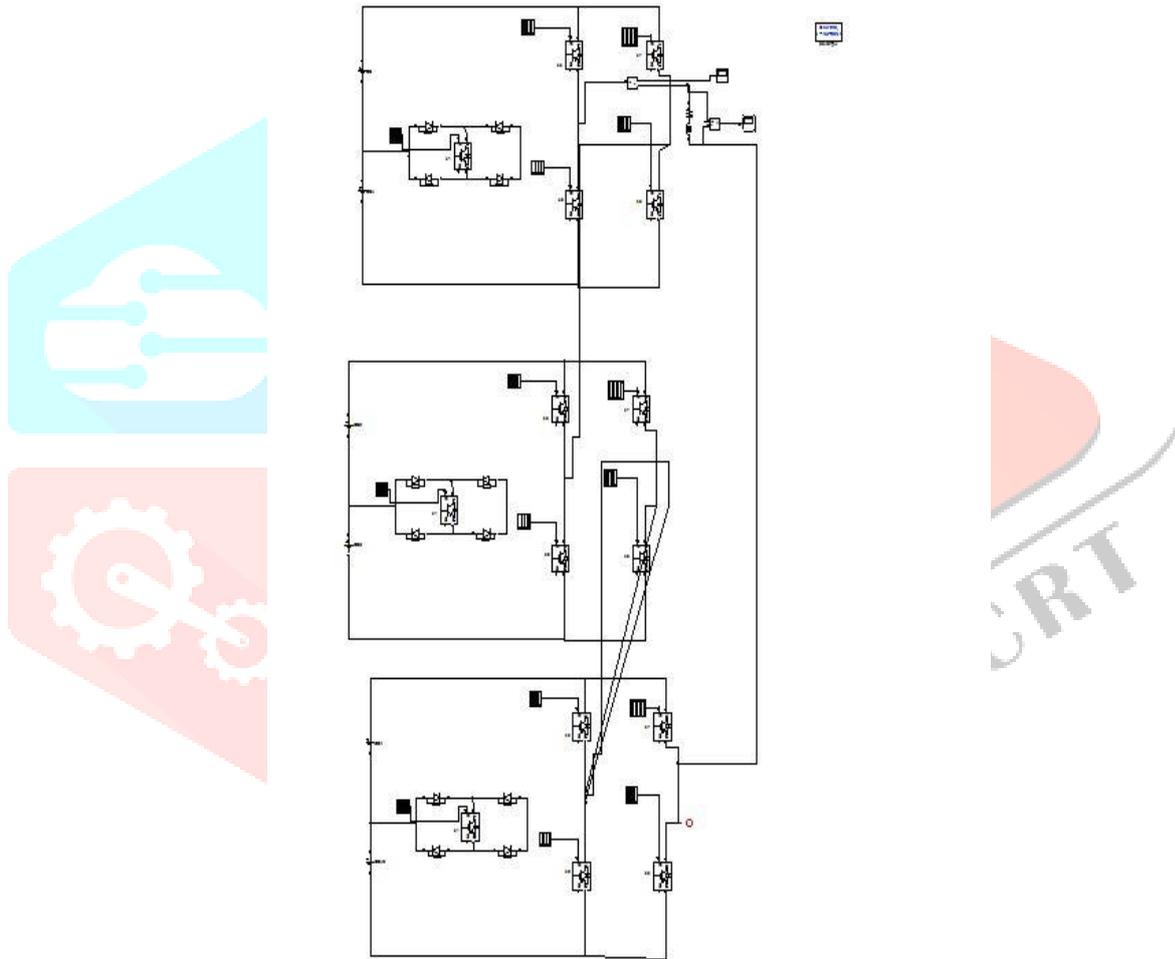


Fig 12 Simulink Diagram of Eleven levels MLI with PWM Technique

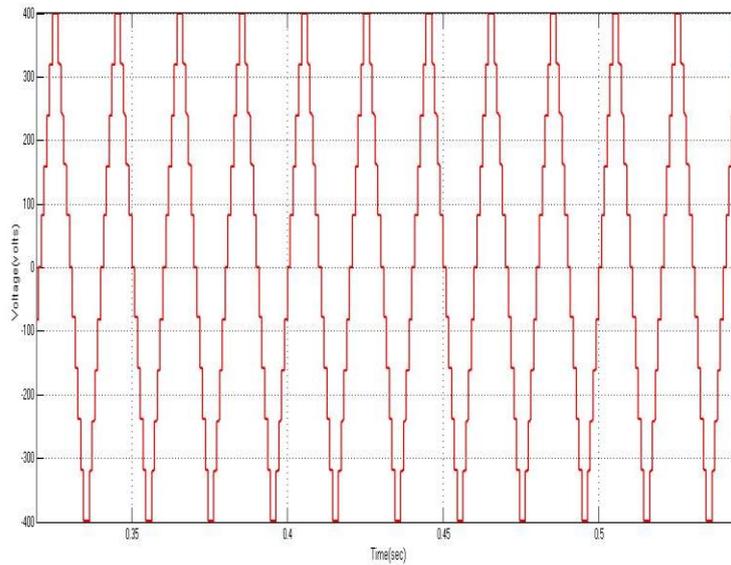


Fig 13 Simulation output voltage waveform of eleven levels MLI with PWM Technique

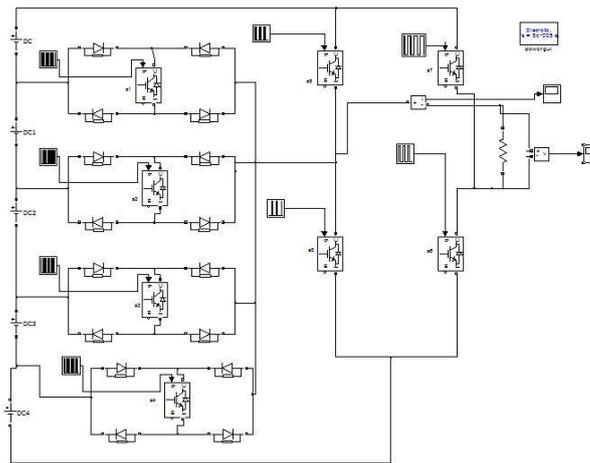


Fig 14 Simulink Diagram of A new eleven levels with reduced switches MLI with PWM Technique



Fig 15 Simulation Output Voltage Waveform of A new eleven levels with reduced switches MLI with PWM Technique

V. CONCLUSION

There is less total harmonic distortion (THD) and fewer hardware components when a cascaded multilevel single-phase inverter is implemented utilising selective harmonic elimination. From the five-level inverter, the implementation assures any required range of levels. There are fewer switches, diodes, DC voltage sources and capacitors in the suggested topologies compared to traditional ones and other newly proposed topologies. The suggested topology is compared to various recently published topologies in a broad variety of ways. It is clear from this comparison that the least amount of IGBTs, capacitors, diodes, and blocking voltages of switches is needed to achieve the greatest number of output voltage levels possible. Finally, Matlab Simulation Simulink was used to simulate and verify the suggested topologies.

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