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Design And Implementation Of Dynamic Approximate Adders

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Abstract: In modern computing systems, achieving a balance between accuracy and power consumption is crucial. As technology gets smaller, it becomes harder for traditional methods to work efficiently. This is applicable even in tasks like videos, signal processing, where exact accuracy is not always needed. So, we go for approximate adders for applications in which accuracy is not significant but there is a need for reduced power consumption and delay. Approximate adders often skip some computations to achieve better performance in terms of energy efficiency and speed.

The project focuses on the designing of exact mirror adder, two types of approximate adders single exact single approximate adder (SESA) and single exact dual approximate adder (SEDA) circuit using 18nm FinFET technology. These circuits are evaluated using the Cadence virtuoso tool. SESA and SEDA have two modes of operation, exact mode for accuracy of the adder and approximate mode for low-power consumption. Using SESA and SEDA, modes can be shifted easily and also allow to vary the amount of approximation.To demonstrate the practical utility of the adders, applied SESA and SEDA architectures in two key application areas: image enhancement and checksum generation.

Index Terms - Single Exact Single Approximate(SESA)Adders ,Single Exact Dual Approximate(SEDA)Adders, Power Gating, Image Enhacement Applications

I. INTRODUCTION

The rapid growth of digital applications, there is a constant need for faster and more energy-efficient computing. Many modern technologies, such as artificial intelligence, image processing, and Internet of Things (IoT) devices, require high-speed arithmetic operations but do not always need perfect accuracy. This has led to the development of approximate computing**,** where small errors in computation are acceptable in exchange for significant improvements in power efficiency, processing speed, and circuit size.Traditional adders ensure precise calculations but often consume more power and require complex logic. Approximate adders, on the other hand, simplify these computations by reducing the number of logic gates, leading to faster and more efficient circuits. However, designing an effective approximate adder involves balancing accuracy with hardware performance.The results demonstrate that SESAA and SEDAA architectures outperform conventional designs in terms of energy efficiency while maintaining acceptable levels of accuracy, making them well-suited for modern low-power and high-performance computing environments.One of the most critical arithmetic components in digital systems is the adder, as it is heavily used in processing elements such as ALU s (Arithmetic Logic Units), DSP blocks, and neural processing units. As a result, a large body of research has focused on developing approximate adders that offer a trade-off between accuracy and efficiency.

1.1. EMA:EXACT MIRROR ADDERS

The Exact Mirror Adder (EMA) is a type of full adder that uses a mirror logic design to perform accurate binary addition. Unlike approximate adders, which deliberately introduce small errors to reduce power and area, the EMA performs addition operations with full accuracy, making it suitable for applications where precision is essential.

Functionally, the EMA computes the sum and carry using the standard Boolean expressions:

Sum = A ⊕B ⊕Cin

Carry-out (Cout) = (A·B) + (B·Cin) + (A·Cin)

While the EMA may not offer the extreme power and area savings of approximate adders, it provides a good trade-off for designs that require exact results with some concern for layout efficiency.A typical EMA design uses around 28 transistors, providing a fully functional and accurate solution without excessive hardware overhead.

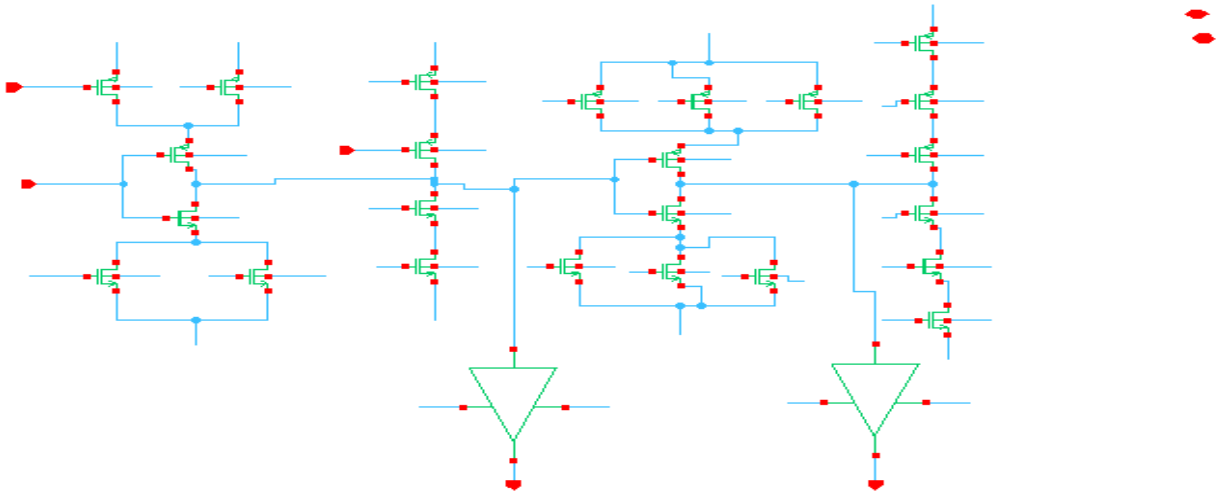

Fig. 1.1. Circuit diagram of exact mirror adder.

In the context of hybrid or configurable adders such as Single Exact, Single Approximate Adders (SESAA) and Single Exact, Dual Approximate Adders (SEDAA), the EMA plays a critical role. It serves as the exact computation core, ensuring correct results when accuracy is necessary, while the approximate counterparts handle less critical computations. This combination allows for dynamic control over power and accuracy, making the EMA a foundational component in energy-efficient, error-resilient arithmetic designs

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Table 1.1. Functional table of exact mirror adder.

INPUTS			OUTPUTS	
a	b	c_{in}	sum	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

II. SESA: SINGLE EXACT SINGLE APPROXIMATE ADDERS

A Single Exact Single Approximate (SESA) adder is a type of hybrid digital adder that combines both accurate and approximate computation strategies within a single adder unit. In this design, one of the output components typically the sum output is computed exactly, while the other output the carry is approximated. This approach allows for a balance between maintaining computational accuracy and achieving improvements in hardware efficiency.

The primary motivation behind SESA adders is to reduce power consumption, area, and delay in digital circuits, especially in applications where perfect accuracy is not always necessary.The exact sum is computed using traditional logic like the XOR of the inputs (A ⊕B ⊕Cin), ensuring correctness where it matters most. The carry output, on the other hand, is generated using an approximate method, which may ignore certain input dependencies (like Cin) to simplify logic gates. This trade-off is what makes SESA adders an attractive choice in the design of energy-efficient arithmetic units.

2.1 SESA1 Adder

The SESA1 adder, or Single Exact Single Approximate Adder – Type 1, is a specific implementation of the hybrid adder concept where the sum output is computed exactly, and the carry output is approximated using a simplified logic function. In this design, the sum (Sum) is generated in the same way as in a traditional full adder using the XOR operation: Sum = A ⊕B ⊕Cin. This ensures that the most visible part of the computation the sum bit—is always accurate, preserving result integrity.However, to reduce hardware complexity and power consumption, the carry output (Cout) is approximated. In the SESA1 adder, the carry is not calculated using the full majority function. Instead, it may use a simpler logic expression such as Cout = A · B, which ignores the Cin input. This significantly reduces the number of logic gates required, lowering both energy usage and delay.

The SESA1 adder is particularly useful in error-tolerant applications where minor inaccuracies in carry propagation do not significantly affect the overall system behaviour. Examples include image processing, neural networks, and other approximate computing domains. By keeping the sum exact and simplifying the carry, the SESA1 adder offers a good trade-off between accuracy, speed, and resource efficiency.

2.2 SESA2 Adder

The SESA2 adder, or Single Exact Single Approximate Adder – Type 2, is another variant of the hybrid adder family that aims to optimize digital arithmetic by balancing accuracy with hardware efficiency. Like SESA1, the sum output (Sum) in SESA2 is computed exactly using the XOR logic: Sum = A ⊕B ⊕Cin, ensuring correct sum results. However, what differentiates SESA2 is the way it approximates the carry output (Cout). Instead of using only A · B as in SESA1, SESA2 uses a different simplified logic, such as Cout = A + B (logical OR or some other approximation), which still avoids the full carry computation but considers more input conditions than SESA1.

This design allows for a slightly more accurate carry approximation than SESA1 while still saving on hardware resources like gate count and power. As with other approximate adders, SESA2 is well-suited for applications that can tolerate small computational errors, such as image processing, data analytics, or approximate computing in embedded systems. The SESA2 adder offers a flexible trade-off between precision and performance, depending on the application's tolerance to error.

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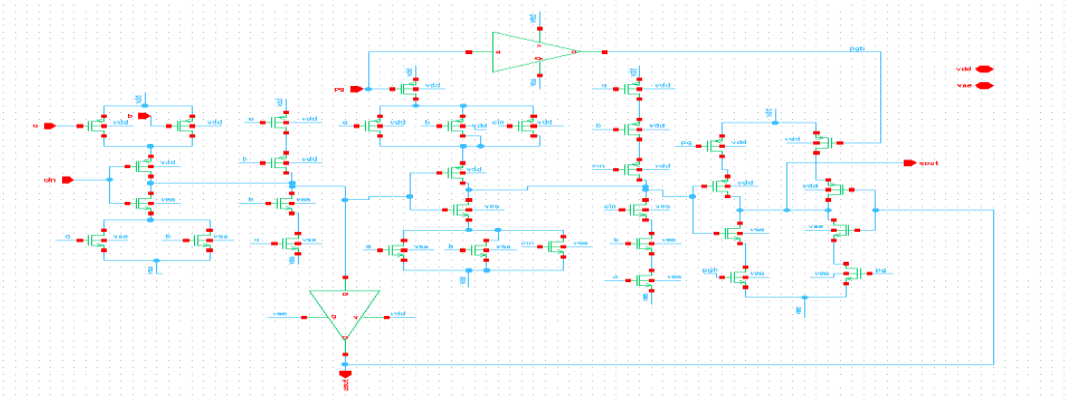

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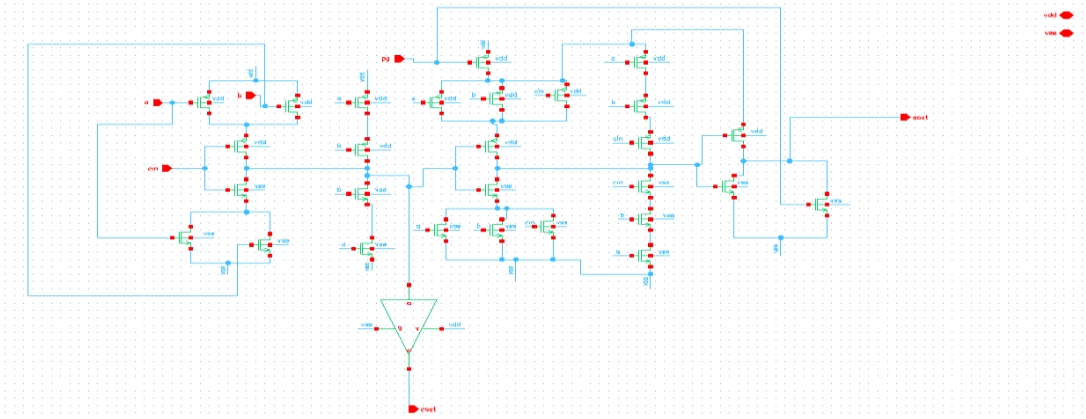

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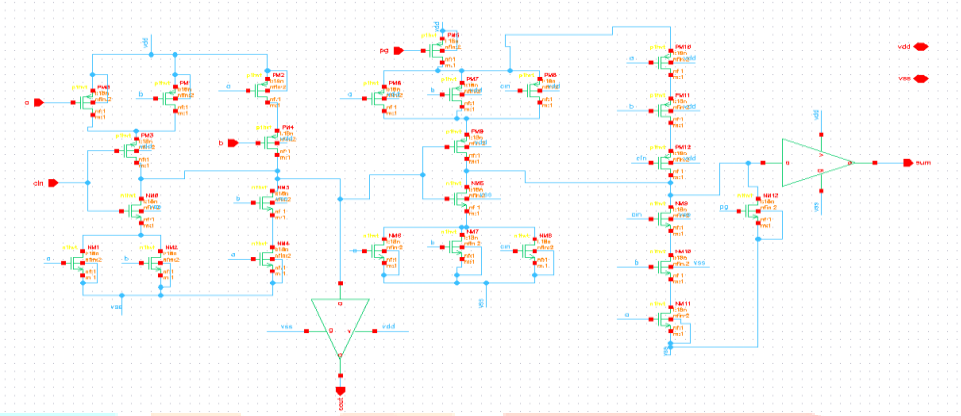


(c)

Fig. 2.1. Circuit diagram of (a) SESA1, (b) SESA2, (c) SESA3

2.3 SESA3 Adder

The SESA3 adder, or Single Exact Single Approximate Adder – Type 3, is a variation of hybrid adders designed to offer a unique balance between computational accuracy and efficiency. Like other SESA variants, SESA3 computes the sum output (Sum) exactly using the full XOR-based. This guarantees that the result of the addition, which is most visible in many applications, remains correct.

What makes SESA3 different from SESA1 and SESA2 is its carry approximation strategy. In SESA3, the carry output (Cout) is approximated using a different logic simplification, such as Cout = B · Cin or another reduced form that deliberately excludes one or more input conditions. This method further simplifies the carry logic when compared to SESA2, often leading to even greater savings in power, delay, and hardware resources, but possibly at the cost of slightly more frequent carry errors.

SESA3 adders are ideal for error-resilient systems where exact carry output is not critical, and resource constraints are a higher priority. Applications such as real-time image filters, audio processing, and machine learning inference tasks can greatly benefit from the low-power and high-speed advantages of SESA3 while tolerating its minor inaccuracies.

III. SEDA: SINGLE EXACT DUAL APPROXIMATE ADDERS

The Single Exact Dual Approximate (SEDA) adder is a specialized hybrid adder architecture designed to balance computational accuracy with hardware efficiency. In this design, the sum output (Sum) is computed exactly using traditional full adder logic, ensuring that the primary result of the addition remains correct. This is crucial for applications where the sum must be precise, even if some approximation is allowed in other parts of the operation.

What makes the SEDA adder unique is its use of two carry outputs: one is the exact carry (Cout), calculated using the full majority function logic, and the other is an approximate carry (Cout), which is generated using simplified logic. The approximate carry may be derived from reduced expressions such as A·B or A + B, intentionally ignoring certain inputs like the carry-in to reduce complexity. This dual carry output allows systems to either compare the exact and approximate results or switch between them depending on the application's accuracy or performance needs.

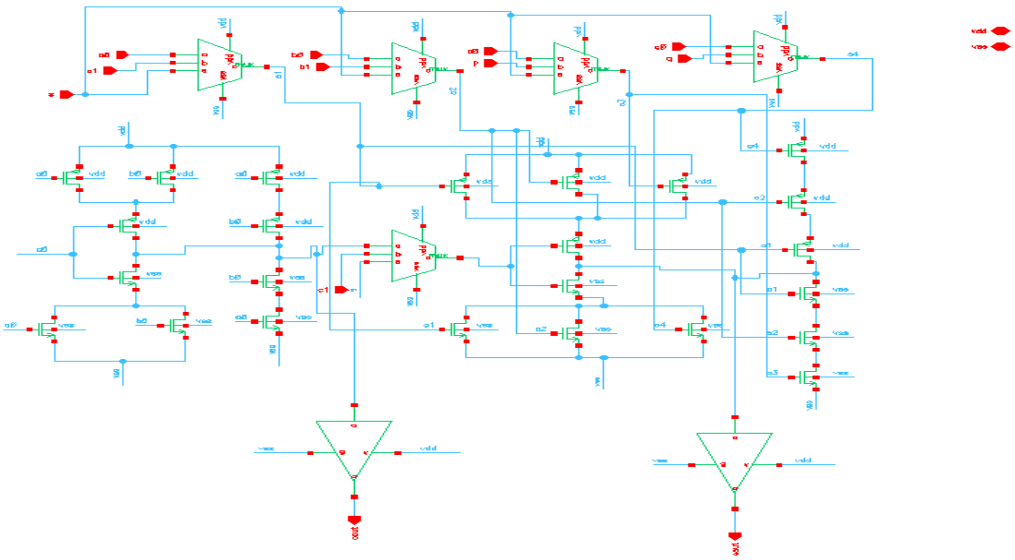
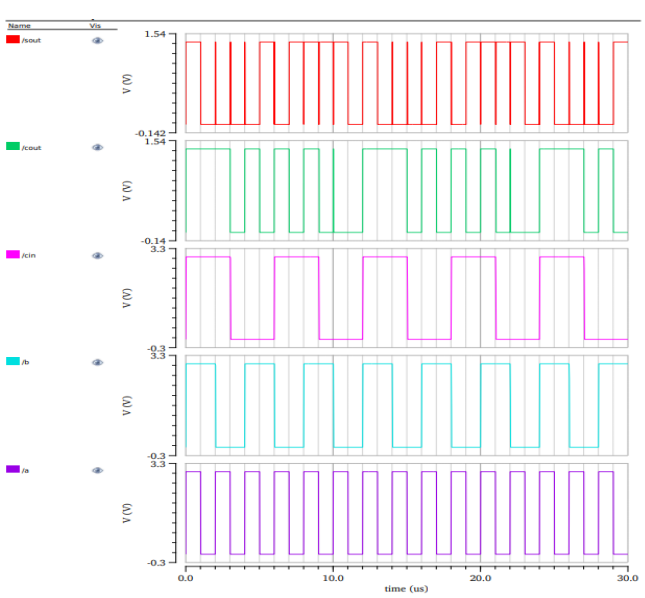


Fig. 3.1. Circuit diagram of SEDA adder

SEDA adders are particularly useful in adaptive and error-tolerant computing systems. They are ideal for tasks like image processing, multimedia applications, and machine learning inference, where perfect accuracy is not always necessary, and reducing power consumption and delay is more critical. By offering both exact and approximate results within the same hardware block, SEDA adders provide designers with the flexibility to optimize energy and speed while maintaining control over computational error.

IV. SIMULATION OF ADDERS

We implemented the proposed approximate adders using 18nm FinFET technology in the Cadence Virtuoso design environment. The simulation results were obtained using detailed schematic and layout-level analysis within this tool. A supply voltage of 0.8 V (typical for FinFET technology) was used during the simulations. The CARRY module, which lies in the critical path of the ripple carry adder, ensuring that both pull-up and pull-down networks conduct equal current. This approach mimics the behavior of inverter, helping to achieve balanced rise and fall delays. In contrast, the SUM module was minimum sized, since it is not part of the critical timing path, allowing for area and power optimization without affecting overall speed. The use of FinFET devices in 18nm technology further enhances performance and reduces leakage, making this implementation suitable for low-power and high-speed arithmetic circuits.



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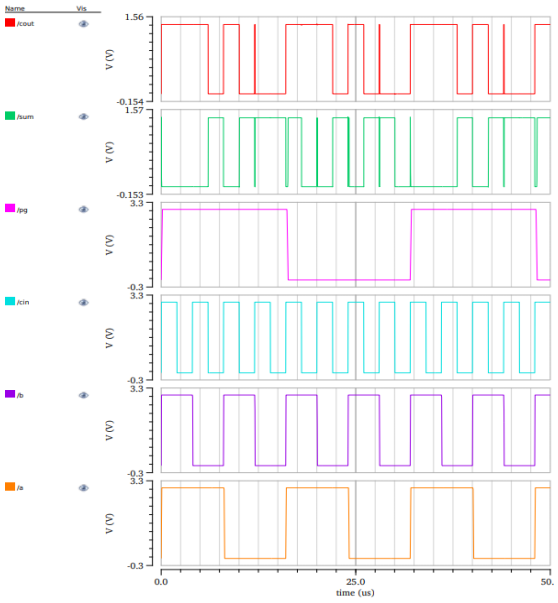

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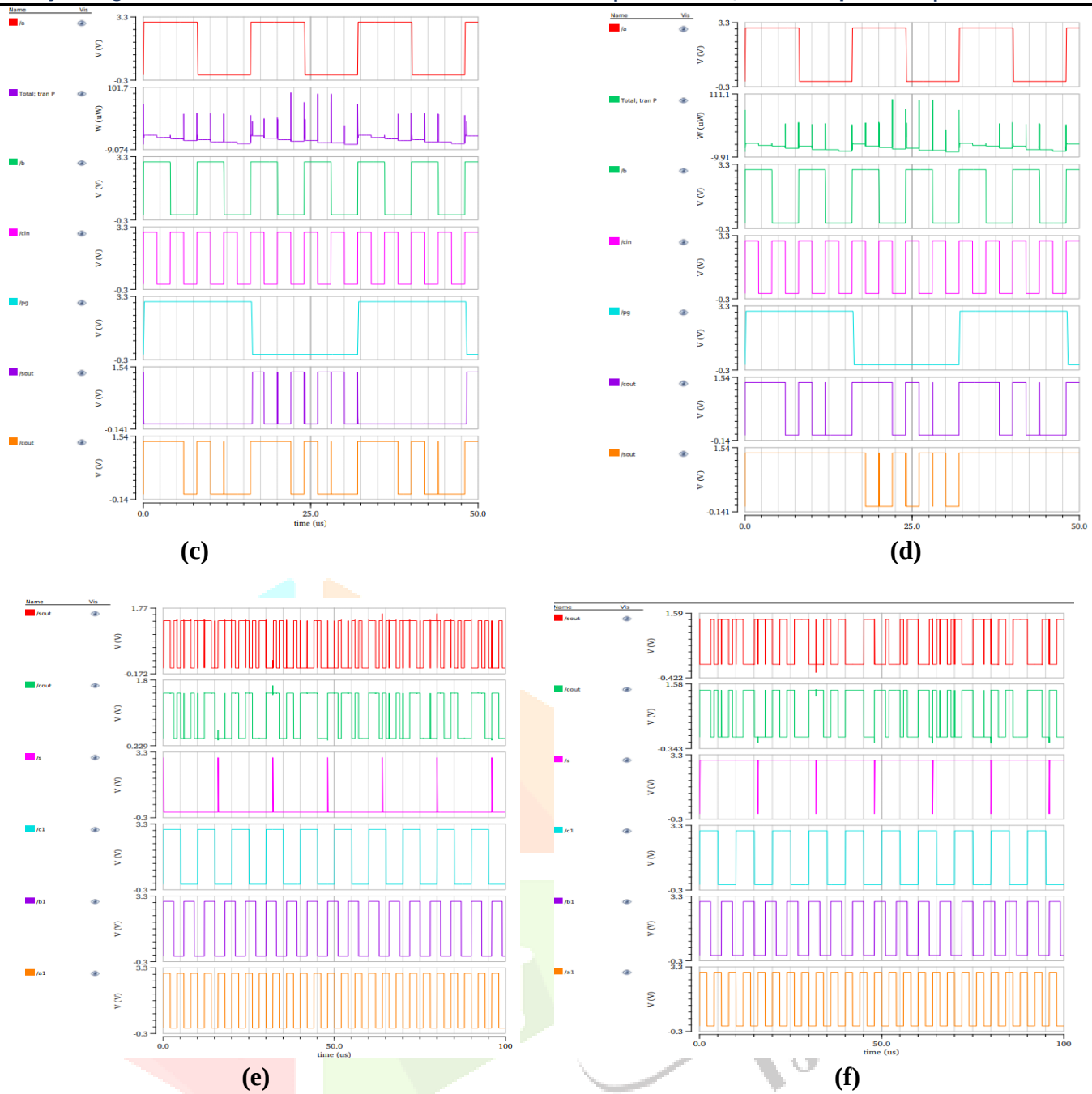


Fig. 4.1. Functional verification of (a) EMA, (b) SESA1,

(c) SESA2, (d) SESA3, (e) SEDA (exact), (f) SEDA (approx.)

Table 4.1. Average power Values (FinFET and CMOS)

Adder Circuit	Average power (in watts)	
	FinFET	CMOS
EMA	7.02E-6	11.07E-6
SESA1	9.08E-6	13.64E-6
SESA2	8.07E-6	13.88E-6
SESA3	8.34E-6	14.51E-6
SEDA	6.82E-6	10.12E-6

Table 4.2.Delay values (FinFET & CMOS)

Adder Circuit	Average power (in watts)		Delay(in seconds)					
			FinFET			CMOS		
	FinFET	CMOS	A- sout A- cout	B-sout B-cout	C-sout C-cout	A- sout A- cout	B-sout B-cout	C-sout C-cout
EMA	7.021E-6	11.07E-6	2.756E-9 3.016E-6	1.02E-9 3.015E-6	0.710E-9 3.013E-6	4.688E-9 3.009E-6	2.176E-9 3.012E-6	2.312E-9 3.016E-6
SESA1	9.085E-6	13.64E-6	10.19E-9 6.017E-6	0.205E-9 6.026E-6	3.811E-9 6.031E-6	2.999E-6 6.017E-6	3.008E-6 6.026E-6	3.013E-6 6.031E-6
SESA2	8.07E-6	13.885E-6	10.20E-9 6.017E-6	0.855E-9 6.026E-6	3.800E-9 6.031E-6	1.984E-6 6.017E-6	1.993E-6 6.026E-6	1.998E-6 6.031E-6
SESA3	8.348E-6	14.51E-6	10.19E-9 6.017E-6	0.867E-9 6.026E-6	3.805E-9 6.031E-6	2.999E-6 6.017E-6	3.009E-6 6.026E-6	3.013E-6 6.031E-6
SEDA	6.82E-6	10.12E-6	19.91E-9 6.017E-6	15.25E-9 6.026E-6	10.58E-9 6.031E-6	7.189E-6 6.017E-6	6.565E-6 6.026E-6	5.697E-6 6.031E-6

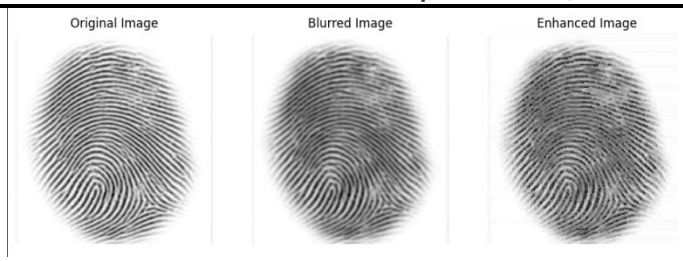
- FinFET consumes significantly less power than CMOS across all adders.
- EMA in FinFET (7.021E-6) compared to CMOS (11.07E-6) demonstrates approximately 36.5% higher power efficiency.
- SEDA, with the lowest power consumption (6.82E-6 in FinFET), is the most efficient choice for low-power applications.
- SEDA in FinFET (6.82E-6) achieves optimal energy efficiency, making it ideal for power-constrained systems.
- EMA in FinFET (~2.756E-9 s delay) delivers superior speed, ensuring high-performance computation.
- EMA or SESA3 in FinFET provides a well-balanced trade-off between power efficiency and computational speed.

V. EVALUATION FOR APPLICATIONS

The effectiveness of our proposed approximate adder designs, we applied them in a real-world scenario—image processing, specifically focusing on enhancing blurred images. We implemented five different adder architectures: Exact Majority Adder (EMA), SESA1, SESA2, SESA3, and SEDA, and evaluated their performance by observing the visual quality of the processed images. The idea was to see how well each adder performed when integrated into a basic image enhancement operation, where arithmetic accuracy can impact the clarity of the final image.During testing, we found that the images processed using EMA and SESA1 adders appeared relatively blurred and less defined, due to the higher degree of approximation in their carry logic.

This level of inaccuracy caused minor distortions in the pixel values, which affected the overall image sharpness. SESA2 and SESA3 produced noticeably better results, with clearer details and improved sharpness, suggesting that their slightly refined carry logic improved computational accuracy while still saving power and area.However, the most significant improvement was observed with the SEDA adder. Images processed using SEDA were sharper, clearer, and visually closer to the original high-quality image. This is because SEDA maintains an exact sum output and utilizes both exact and approximate carry paths, allowing it to strike a better balance between accuracy and efficiency. The additional carry output helps preserve image details, especially in edge areas where small errors can lead to visible artifacts.

(a)



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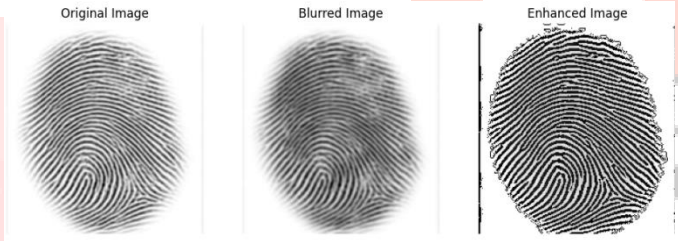

(e)

Fig. 5. (a)EMA, (b) SESA1, (c) SESA2, (d) SESA3,(e) SEDA

Overall, the evaluation shows that while simpler adders like EMA and SESA1 are useful for energy-saving applications, SEDA is the most effective choice for image processing tasks, especially where visual clarity and detail preservation are important. This demonstrates that approximate computing, when designed smartly like in SEDA, can be highly effective for power-efficient image processing without sacrificing much in terms of output quality.

V. CONCULSION

We analyzed and compared various adder architectures, including Single Exact, Single Approximate, and Dual Approximate Adders. Our study highlights the trade-offs between power consumption, delay, and accuracy in computational tasks. Approximate adders provide significant benefits in power-efficient applications by reducing computational complexity while maintaining an acceptable level of accuracy. These adders demonstrate significant improvements is image processing. Approximate adders, particularly in dual approximate configurations, enhance image-related tasks by accelerating computations in applications such as image filtering, edge detection, and compression algorithms.

The inherent tolerance of image processing applications to minor inaccuracies makes these adders an excellent choice for reducing power consumption while maintaining visual quality. Overall, the integration of approximate adders in hardware accelerators and digital signal processing circuits can lead to efficient, high-performance, and low-power solutions, particularly in AI-driven image enhancement and real-time processing applications. Future research can explore further optimizations to balance accuracy and efficiency, expanding their usability across various domains.