IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

# DESIGN OF LOW POWER HIGH SPEED BOOTH MULTIPLIER USING GDI BASED CARRY BYPASS ADDER

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***Abstract:*** In this project, low power consumption and high speed are some of the most important criteria for the fabrication of DSP systems and any high- performance systems. Based on Booth Algorithms, a modified booth multiplier structure is designed by implementing a carry bypass adder. The carry bypass adder is designed by using Gate Diffusion Input (GDI) method. Optimizing the speed and power of the adder is a major design issue. However, area and speed are usually conflicting constraints so that improving speed results mostly in larger areas**.**

***Index Terms*** **– Booth multiplier, GDI Logic, Tanner EDA, VLSI**

## I. INTRODUCTION

Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining hundreds of thousands of transistors or devices into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. Before the introduction of VLSI technology most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. VLSI lets IC designers add all of these into one chip. Multipliers play an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets – high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI implementation. The common multiplication method is "add and shift" algorithm. In parallel multipliers number of partial products to be added is the main parameter that determines the performance of the multiplier. To reduce the number of partial products to be added, Modified Booth algorithm is one of the most popular algorithms. In our project we introduce the booth multiplier with GDI logic to compare them in terms of speed, power and combination of these metrics.

Power consumption refers to the electrical energy per unit time, supplied to operate something, such as a home appliance. Power consumption is usually measured in units of watts (W) or kilowatts (kW). Power is wasted as heat, vibrations and/or electromagnetic radiation. For example, a light bulb does not only convert electric power into light; it also makes some heat. Power consumption is of great importance in digital systems. The battery life of portable systems such as cell phones and laptop computers are limited by power consumption. Digital systems draw both dynamic and static power. Dynamic power is the power used to charge capacitance as signals change between 0 and 1. Static power is the power used even when signals do not change and the system is idle. CMOS devices have very low static power consumption, which is the result of leakage current. But when switching at a high frequency, dynamic power consumption can contribute significantly to overall power consumption. Charging and discharging a capacitive output load further increases this dynamic power consumption.

A delay used to separate the occurrence of two events, especially in an electronic device. It may be measured in terms of time, money, or a combination there of.

OBJECTIVE

- To propose GDI technique-based carry bypass adder to improve power consumption and delay.
- To implement the proposed carry bypass adder in the booth multiplier.
- To reduce the power consumption and to improve speed and overall performance of the booth multiplier using the proposed technique.

## II. RELATED WORK

### A. Hybrid Carry Look-ahead Adder

The existing method of hybrid carry look-ahead adder. This method is divided into three stages as like hierarchical carry look-ahead adder. The Fig.2.1 show the design of Hybrid CLA. In stage one, accept the two n-bit number of inputs and produce propagate and generator value. One more advantage is that there is no need to generate the carry propagate (Pout) and carry generate (Gout) signals. Here the carry of the whole design is generated in the bottom stage of the structure. By this method the area of the design is reduced. So, this is one way to design high speed and less area carry look-ahead adder design

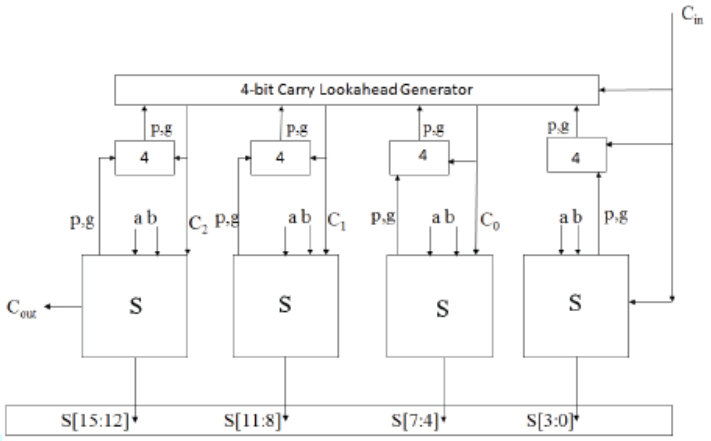


**Figure 2.1** Block diagram of a hybrid carry look-ahead adder

**OPERATION**

P: an indicator whether the carry was propagated to the component. In other words, the carry is propagated through the entire component if and only if it was propagated through every one of the components from the previous stage. The equation (1) is for the 4-bit module.

- P = P0P1P2P3 (1)

G: an indicator whether the carry was generated to the component. In other words, the carry is generated through the entire component if and only if it was generated through every one of the components from the previous stage. The equation (2) is for the 4-bit module.

- G= P1P2P3 G0 + G1 P2P3 + G2P3 + G3 (2)

### B. Booth Multiplier

In Existing system, a novel area efficient and high-speed parallel multiplier and accumulator based modified booth algorithm architecture. The results of accumulation and multiplication stages clubbed using hybrid reduction through Full adder and Carry Look ahead Adder. This helps us to attain more efficiency and speed. In addition, the normal full adder in the CSA is replaced by a new reversible logic gate. The circuit is simulated using Verilog HDL and synthesized in Xilinx ISE Simulator The Block diagram for Booth multiplier as shown in Figure 2.2.

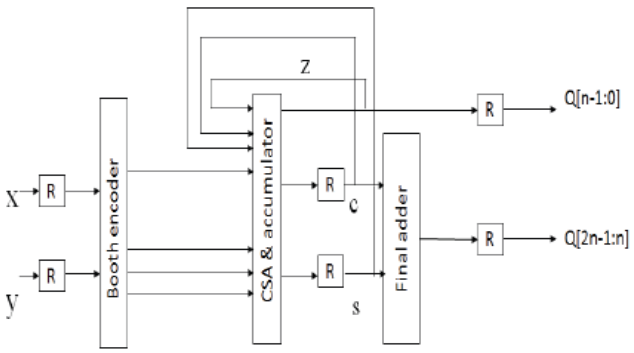


**Figure 2.2** Block diagram of Booth Multiplier

**CONDITIONS**

- If Q0, Q-1 are same i.e., 00 or 11 then, perform arithmetic right shift by 1 bit.
- If Q0, Q-1 = 10 then perform,

$$A \leftarrow A-M$$

- And then perform arithmetic right shift.
- If Q0, Q-1 = 01 then perform

$$A \leftarrow A+M$$

- And then perform arithmetic right shift.

### *C.* Carry Bypass Adder

The carry bypass adder is also called carry skip adder. In the carry bypass adder consists of two full adders, AND gate and one multiplexer. The propagation value of the full adder is given as an input to the AND gate and its output is act as a select line for the multiplexer. To reduce the power, delay and area, GDI technique was implemented on the full adder, the AND gate and finally the multiplexer also. The block diagram for carry bypass adder as shown in Figure 2.3.

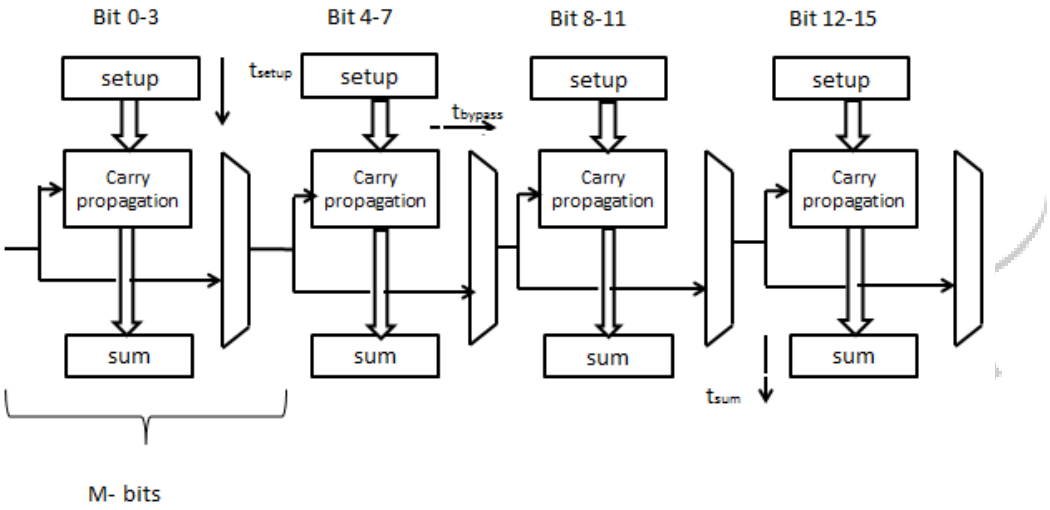


**Figure 2.3** Block diagram of carry bypass adder

$$t_{adder} = t_{setup} + Mt_{carry} + (N/M-1)\, t_{bypass} + (M-1)\, t_{carry} + t_{sum}$$

### D. GDI Logic

GDI method is based on the use of a simple cell. At the first look the design is seems to be like an inverter, but the main differences are

- ✓ GDI consist of three inputs-
- ✓ G (gate input to NMOS/PMOS),
- ✓ P (input to source of PMOS),
- ✓ N (input to source of NMOS).

Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with CMOS inverter.

A simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions. Most of these functions are complex (6- 12 transistors) in CMOS, as well as in standard PTL implementations, but very simple (only 2 transistors per function) in GDI design method.

## III. PROPOSED WORK

### Proposed Booth Multiplier

Design of modified booth encoder and decoder scheme for high performance of parallel multiplier has been proposed. The proposed booth encoder and decoder logic are competitive with the present schemes and shows enhancements in delay. It additionally shows a substantial reduction in area. The 16-bit booth multiplier is designed by booth encoder and booth decoder simulated in tanner tool.

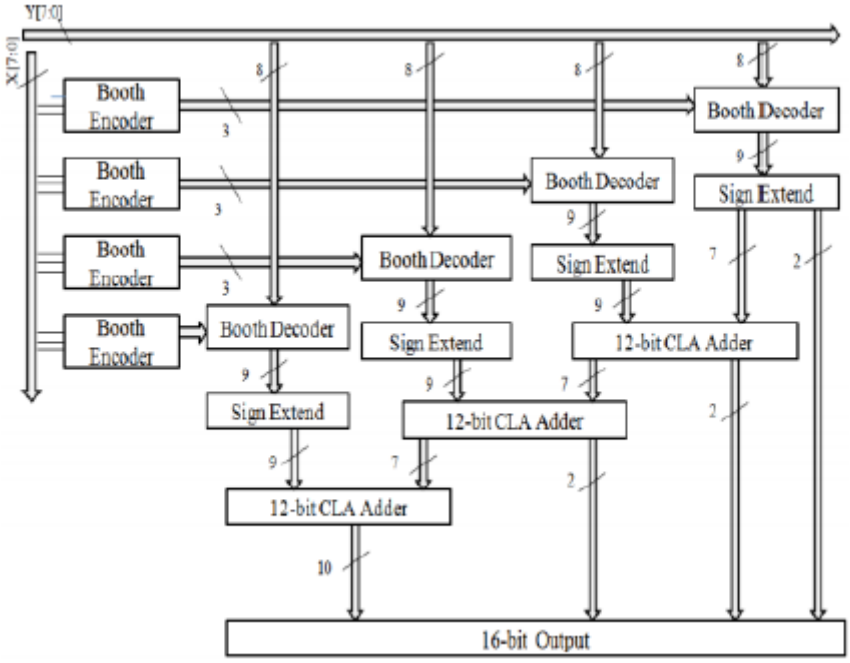


**Figure 3.1** Block diagram for 8-bit booth multiplier

### Proposed Booth Encoder and Booth Decoder

The modified booth encoder, which is implemented using some logic gates. The partial products are generated using the booth decoder. while generating the partial products from the booth decoder, then we followed sign extension prevention. The Schematic diagram for Booth encoder and Booth decoder as shown in Figure 3.2 and 3.3.

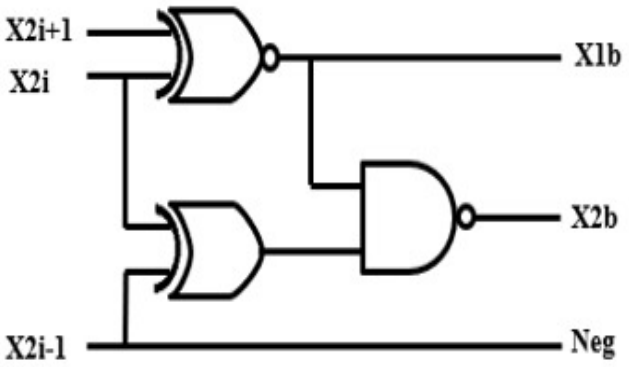


**Fig. 3.2** Schematic diagram for Booth encoder

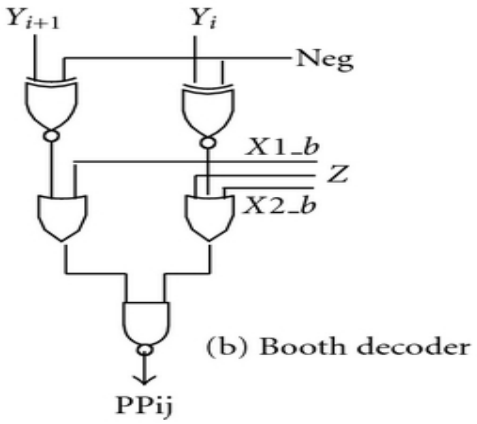


**Fig. 3.3** Schematic diagram for Booth decoder

## IV. RESULT AND DISCUSSION

The booth multiplier is designed using gate diffusion input (GDI) technique-based carry bypass adder and logic gates. The proposed booth multiplier shows a considerable reduction in power consumption and delay. This proficient low power and high-speed booth multiplier is designed using the proposed carry bypass adder for DSP applications.

**Simulation Result for Proposed Carry bypass Adder**

The Schematic diagram for 16-bit carry bypass adder as shown in Figure.4.1

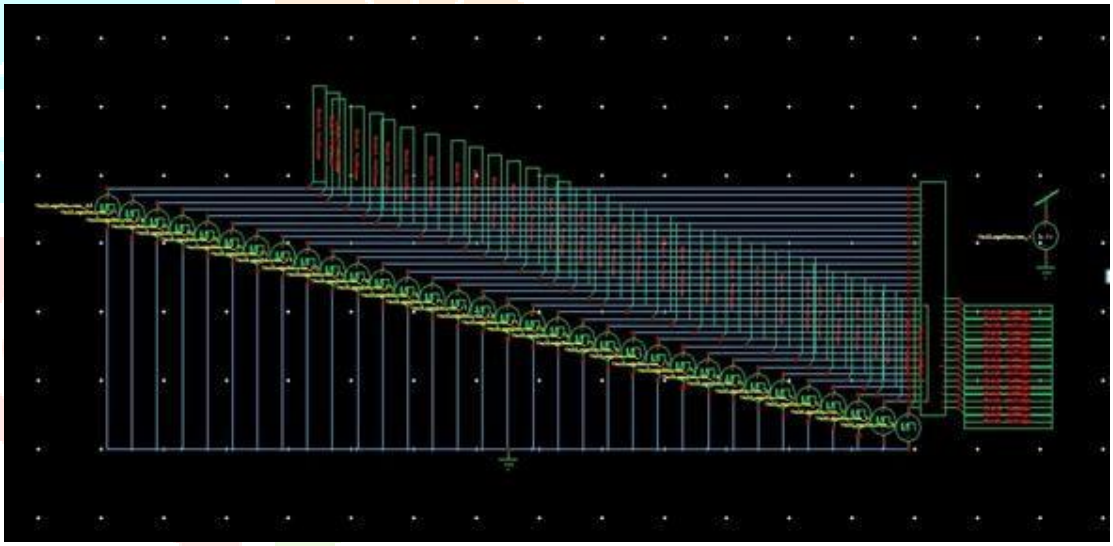

Fig4.1. Schematic diagram for 16-bit carry bypass adder

**Performance Comparison of Proposed Carry Bypass Adder**

Table :1 Performance comparison for various adders

| ADDERS | GDI LOGIC | |
|---|---|---|
| | POWER (m watts) | DELAY (n sec) |
| 8 Bit CLA | 0.26 | 1.93 |
| 8 Bit CBA | 0.01 | 0.16 |
| 8 Bit CSKA | 3.04 | 2.78 |
| 8 Bit CIA | 5.79 | 2.49 |
| 8 Bit KSA | 7.06 | 3.29 |
| 8 Bit HCA | 2.44 | 4.08 |
| 8 Bit BKA | 1.85 | 4.56 |

Table :2 Performance Comparison of carry bypass Adder

| ADDER | WITH GDI TECHNIQUE | |
|---|---|---|
| | POWER (m Watts) | DELAY (ns) |
| 4 BIT CLA | 0.0147 | 19.30 |
| 4 BIT CBA | 0.0144 | 0.016 |
| 8 BIT CLA | 0.0268 | 19.34 |
| 8 BIT CBA | 0.0162 | 0.112 |
| 16 BIT CLA | 0.0977 | 40.58 |
| 16 BIT CBA | 0.0219 | 1.272 |

**Simulation Results for Proposed Booth Multiplier**

***8-bit GDI Based Booth Multiplier***

The Schematic diagram for 8-bit booth multiplier as shown in Figure 4.2

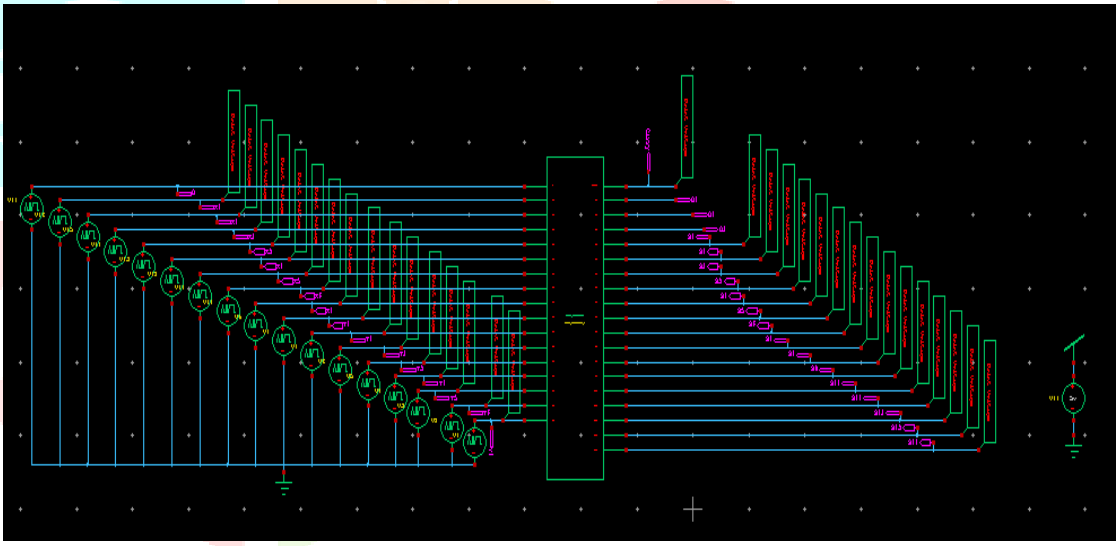

Figure 4.2: Schematic diagram for 8-bit booth multiplier

**Performance Comparison of Booth Multiplier**

Table: 3 Performance Comparison of Booth multiplier

| BOOTH MULTIPLIER | WITHOUT GDI TECHNIQUE | WITH GDI TECHNIQUE |
|---|---|---|

| | POWER (m Watts) | DELAY (ns) | POWER (m Watts) | DELAY (ns) |
|---|---|---|---|---|
| 8-bit | 30 | 28.171 | 0.00384 | 2.1855 |

## CONCLUSION

In this project, a low power and high-speed booth multiplier using GDI technique-based carry bypass adder was designed. Full adder and Multiplexer are the two main peripheral components of the carry bypass adder which were designed using GDI technique for new low power high speed carry bypass adder. Thus, from the simulation results it was observed that the proposed carry bypass adder using GDI Technique provides a low power high speed booth multiplier.

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